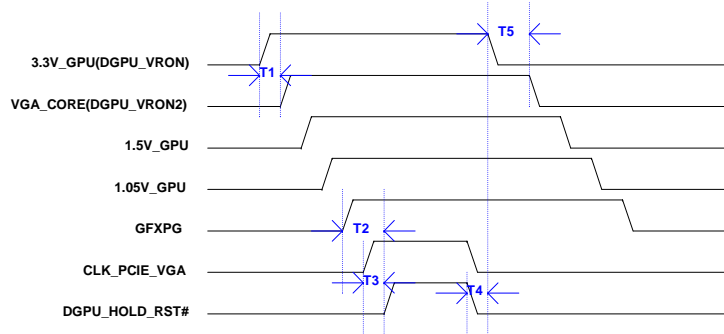


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5	IVB rPGA 1/4(HOST&PCIE)	CPU
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9	PCH 2/6(SATA/RTC/HDA/LPC)	CLG
10	PCH 3/6(PCIE/USB/CLK/NV)	CLG
11	PCH 4/6(GPIO/CPU)	CLG
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25	LVDS/CCD/CRT	LVDS/CCD/CRT
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27	WLAN/UMTS/BT	WLAN/UMTS/BT
28	LAN RTL8111F	LAN RTL8111F
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31	TPM/KB/TP/LED/HOLE	TPM/KB/TP/LED/HOLE
32	EC ITE8518	EC
33	SYSTEM 5V/3V (RT8223PZQW)	PWR
34	VCORE(ISL95836HRTZ-T) QC	PWR
35	DDR3 1.5V(RT8207LZQW)	PWR
36	1.8V_S0(G5173R41U)	PWR
37	1.05V_S0 (TPS51211DSCR)	PWR
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39	VCCSA (G9336ADJTP1U)	PWR
40	VGPU_COR(NCP3218MNR2G)	PWR
41	Discharger	PWR
42	Load SW	PSW
43	Charger (BQ24707RGRR)/DCIN	PWR
44	Change List	

POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States
			ACTIVE IN
VIN	10V~+19V		S0-S5
3V_RTC	+3.0V~+3.3V		S0-G3
3V_S0	+3.3V	S0_ON1	S0
3V_S5	+3.3V	EC	S0-S5
3V_AUX	+3.3V	AC/DC Insert enable	AWLAYS
5V_S0	+5V	S0_ON1	S0
5V_S3	+5V	S3_ON	S0-S3
5V_S5	+5V	EC	S0-S5
5V_AUX	+5V	AC/DC Insert enable	AWLAYS
1.8V_S0	+1.8V	S0_ON2	S0
1.5V_S0	+1.5V	S0_ON2	S0
1.5V_S3	+1.5V	S3_ON	S0-S3
1.05V_S0	+1.05V	S0_ON2	S0
VCCSA	By VID	S0_ON2	S0
CPU_CORE	By VID	VR_ON	S0
VCC_AXG	By VID	VR_ON	S0
3V_LAN	+3.3V	LAN_ON	S0-S5(By WOL)
3V_GPU	+3.3V	DGPU_VRON	Optimus
1.5V_GPU	+1.5V	DGFX_VR_PWRGD	Optimus
1.05V_GPU	+1.05V	DGFX_VR_PWRGD	Optimus
VGA_CORE	By VID	DGPU_VRON1	Optimus

N13P-LP Power ON/OFF Sequence



BIOS/ EC control:

T1:DGPU_VRON to DGPU_VRON2 = 500us

T2:GFXPG to DGPU_HOLD_RST# = 5ms

T3:CLK_PCIE_VGA to DGPU_HOLD_RST# >100us(Spec)

T4:DGPU_HOLD_RST# to DGPU_VRON = 5ms

Note: Clock must be shutdown before 3.3V_GPU

T5:DGPU_VRON to DGPU_VRON2 = 500us

N13P-LP & N13P-GLP Table

	N13P-GLP	N13P-LP
VL3	BLM18P121SN (CX8PG121009)	0ohm_0603 (CS00003J951)

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

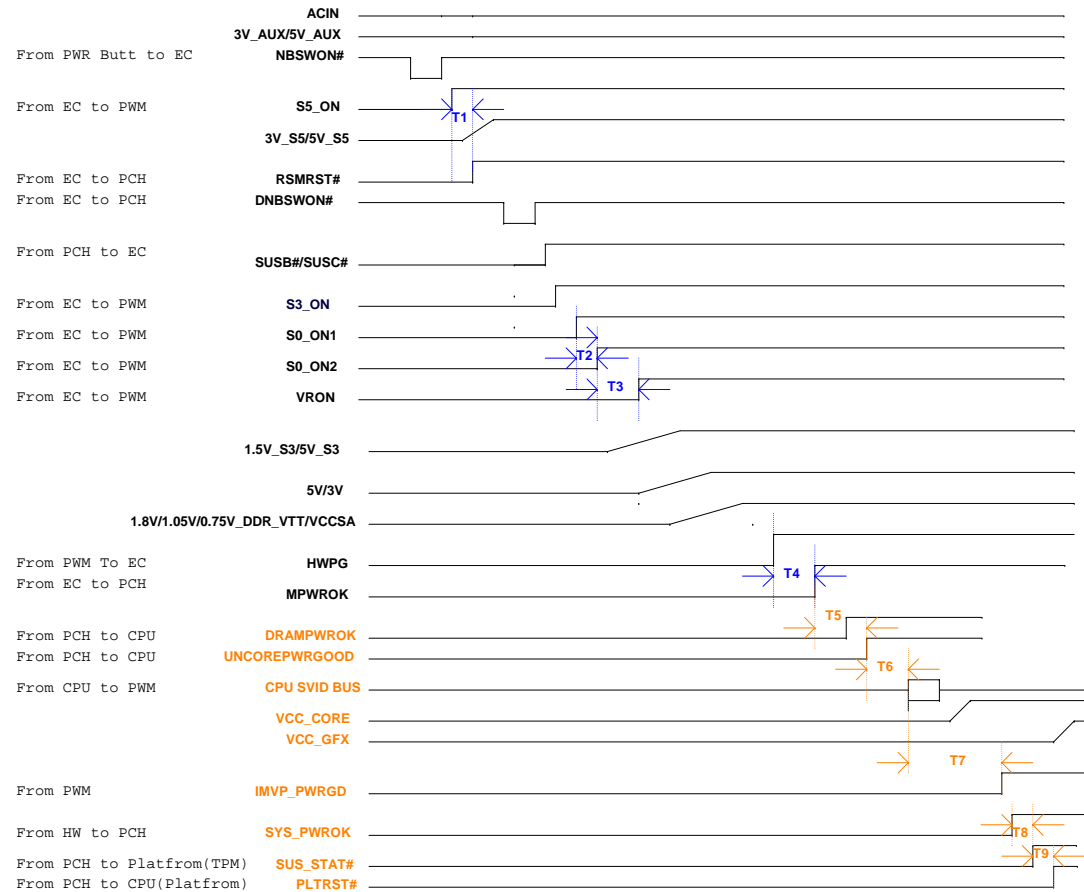
	N13P-GLP	N13P-LP
VR62	10Kohm_0402 (CS31002FB26)	NA

ID2	ID1	ID0	Model
0-R435	0-R438	0-R437	FJ8 UMA
0-R435	0-R438	1-R430	FJ8 Discrete
0-R435	1-R382	0-R437	PH6 UMA(Consumer)
0-R435	1-R382	1-R430	PH6 UMA(Commercial)
1-R384	0-R438	0-R437	PH6 N13P-LP
1-R384	0-R438	1-R430	PH6 N13P-GLP
1-R384	1-R382	0-R437	TBD
1-R384	1-R382	1-R430	TBD

B-29

		GLP 1GB HYN	GLP 1GB SAM	GLP 2GB HYN	GLP 2GB SAM	LP 2GB HYN	LP 2GB SAM
ROM_SCLK	VR44	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR54	CS31502FB24	CS31502FB24	CS31502FB24	CS31502FB24	NA	NA
ROM_SI	VR41	NA	NA	NA	NA	NA	NA
	VR52	CS31502FB24	CS32002FB29	CS33012FB18	CS34532FB18	CS33012FB18	CS34532FB18
ROM_SO	VR43	NA	NA	NA	NA	CS31002FB26	CS31002FB26
	VR53	CS31002FB26	CS31002FB26	CS31002FB26	CS31002FB26	NA	NA
STRAP0	VR51	NA	NA	NA	NA	CS34532FB18	CS34532FB18
	VR55	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	NA	NA
STRAP1	VR46	NA	NA	NA	NA	CS34532FB18	CS34532FB18
	VR56	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS24992FB26	CS24992FB26
STRAP2	VR47	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	NA	NA
	VR57	NA	NA	NA	NA	CS32002FB29	CS32002FB29
STRAP3	VR48	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR58	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	NA	NA
STRAP4	VR50	NA	NA	NA	NA	NA	NA
	VR59	NA	NA	NA	NA	CS34532FB18	CS34532FB18

System Power-ON Sequence



System Power Sequence

EC Control:

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)

T2: S0_ON1 TO S0_ON2 = 500us

T3: S0_ON2 TO VRON = 10ms

T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)

Note:HWPG NEED TO BE HIGH at that time

System:

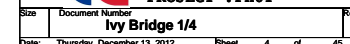
T5: MPWROK to UNCOREPWROK =2ms(Min)

T6: UNCOREPWROK to SVID Packet =500us(Max)

T7: SVID Packet to IMVP_PWRGD =5ms(Max)

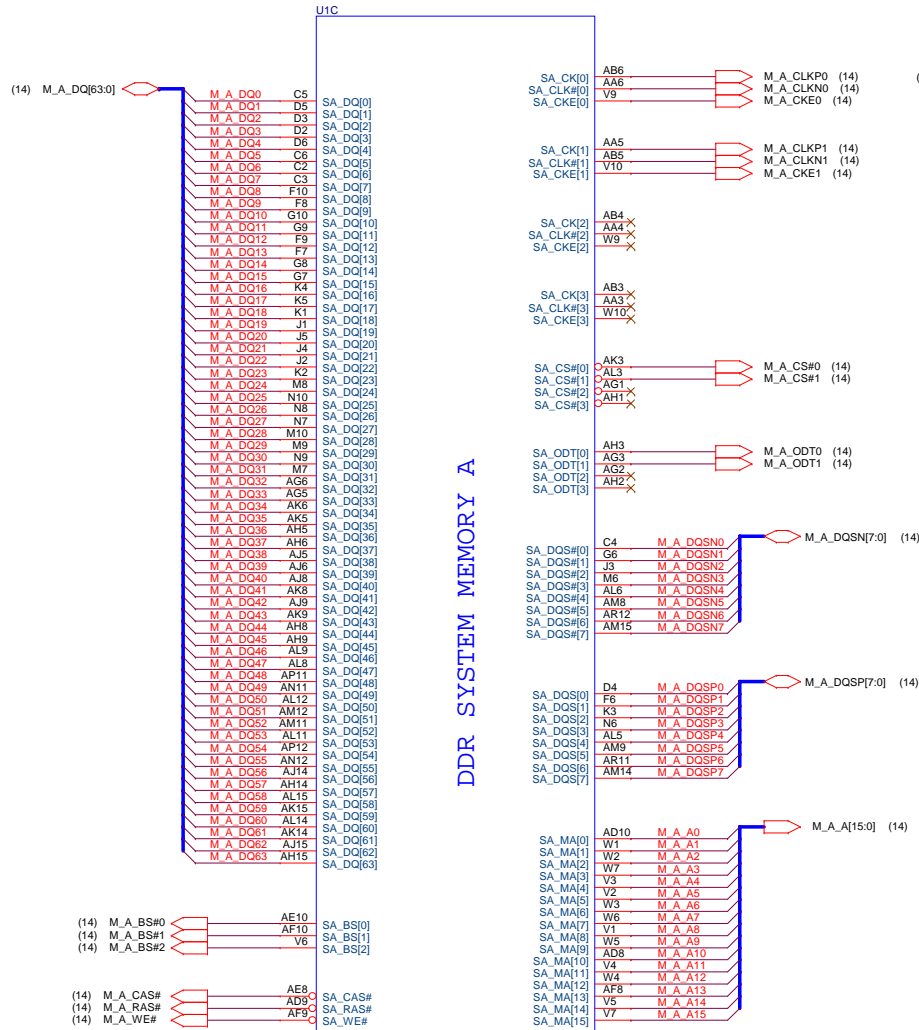
T8: SYS_PWROK to SUS_STAT# =1ms(Min)

T9:SUS_STAT# to PLTRST# =60us(Min)

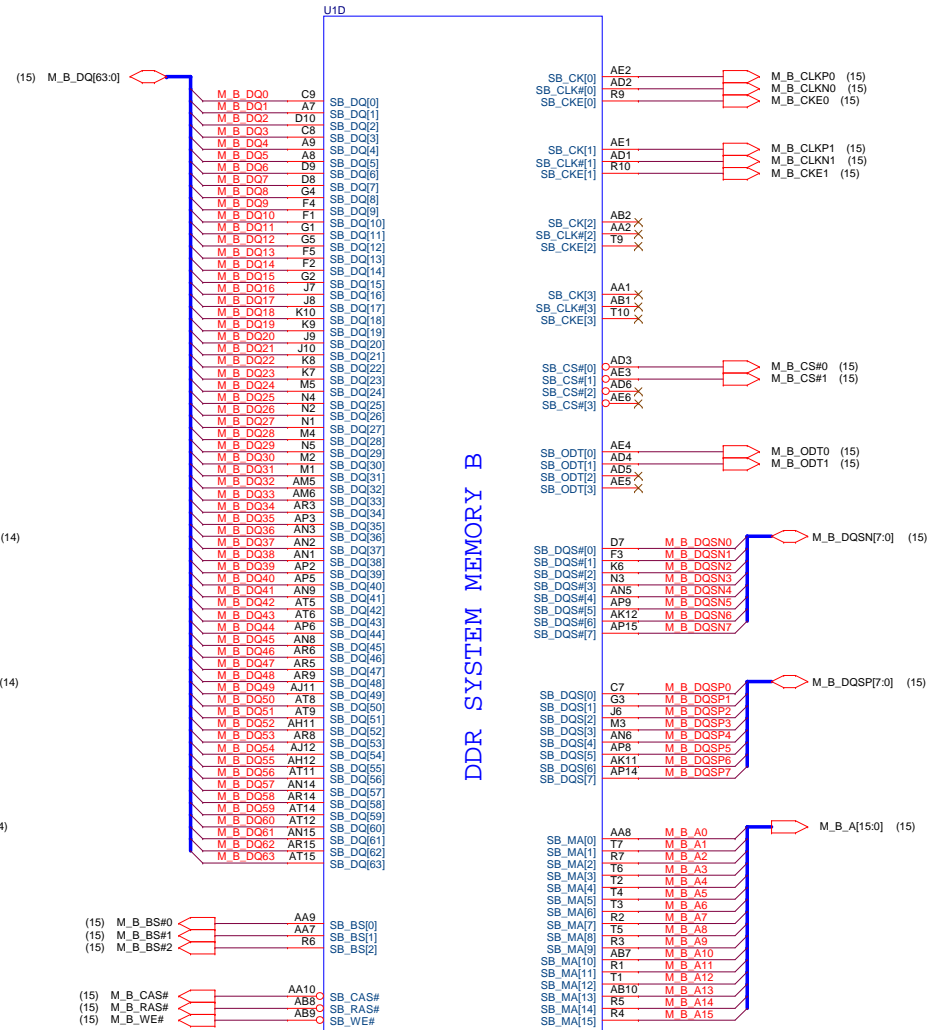


Ivy Bridge Processor (DDR3)

05



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

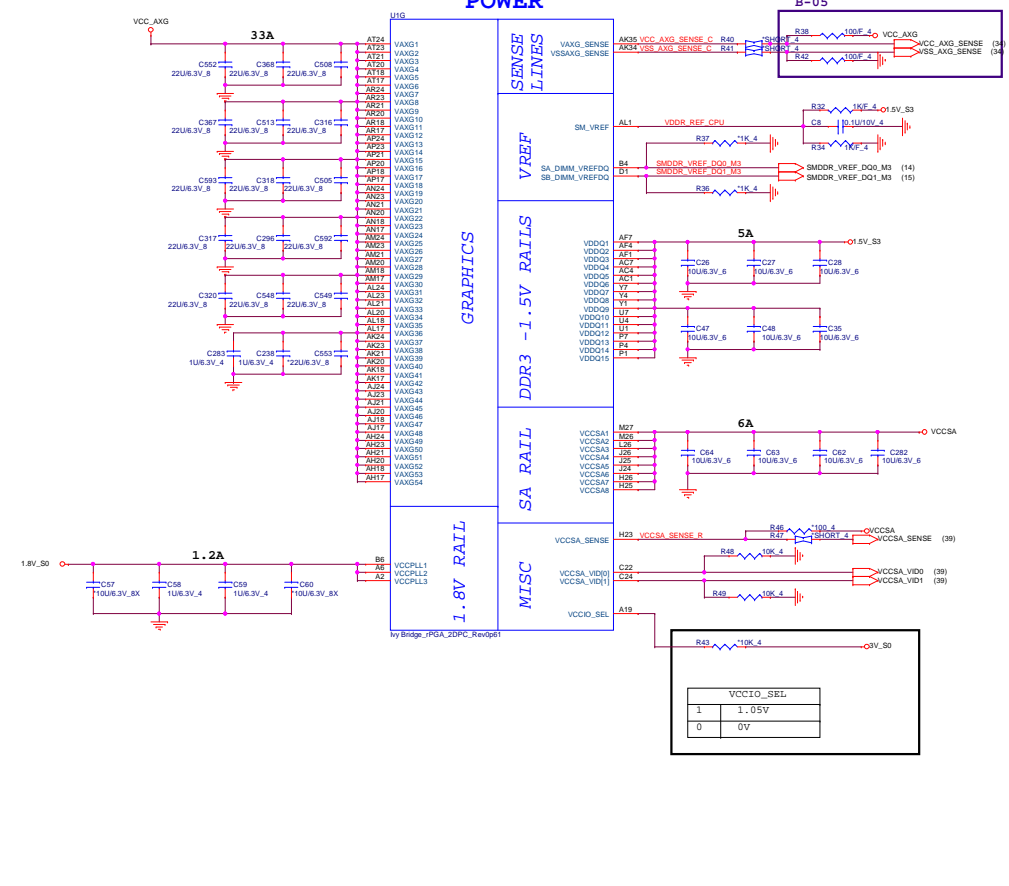
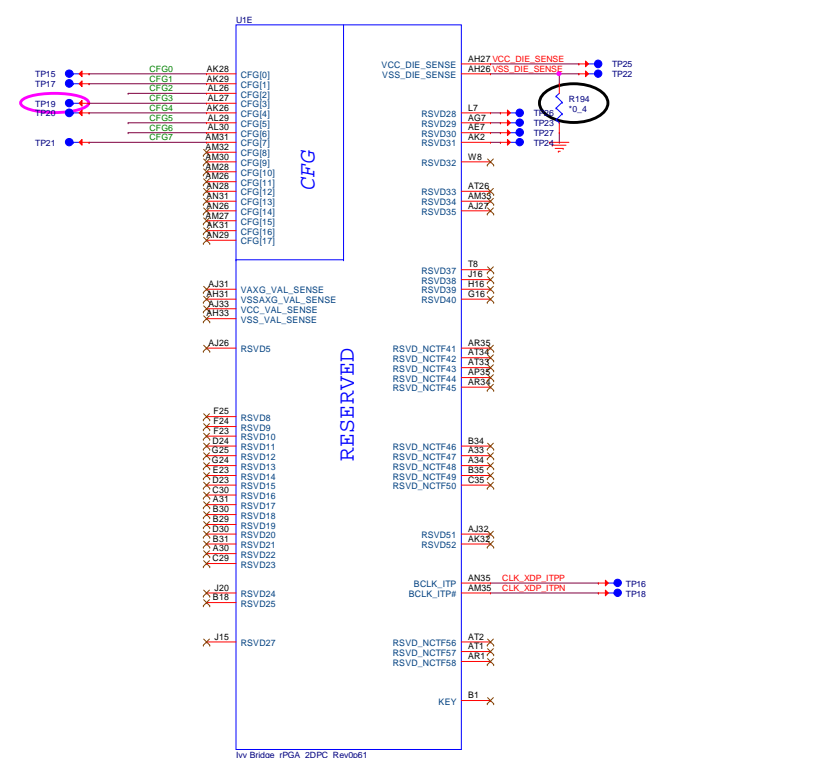
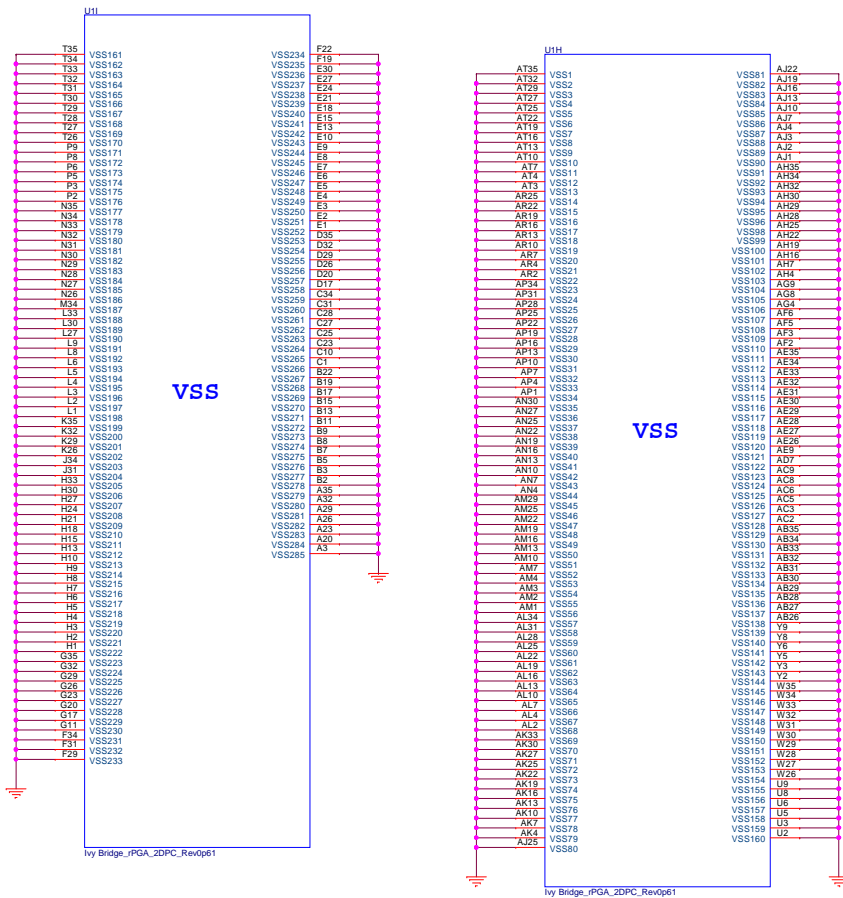


Figure 10 shows the schematic diagram of the VR_SVID interface. It consists of three signal lines:

- H_CPU_SVIDCLK** is connected to **VR_SVID_CLK** (34) via a **75SHORT_4** resistor.
- H_CPU_SVIDDAT** is connected to **VR_SVID_DATA** (34) via a **75SHORT_4** resistor. A **1.05V_S0** voltage source is connected to the **H_CPU_SVIDDAT** line through a resistor **R20** (130F_4).
- H_CPU_SVIDALRT#** is connected to **VR_SVID_ALERT#** (34) via a **75_4** resistor. A **1.05V_S0** voltage source is connected to the **H_CPU_SVIDALRT#** line through a resistor **R61** (75_4).

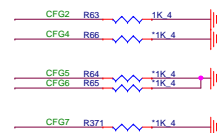
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

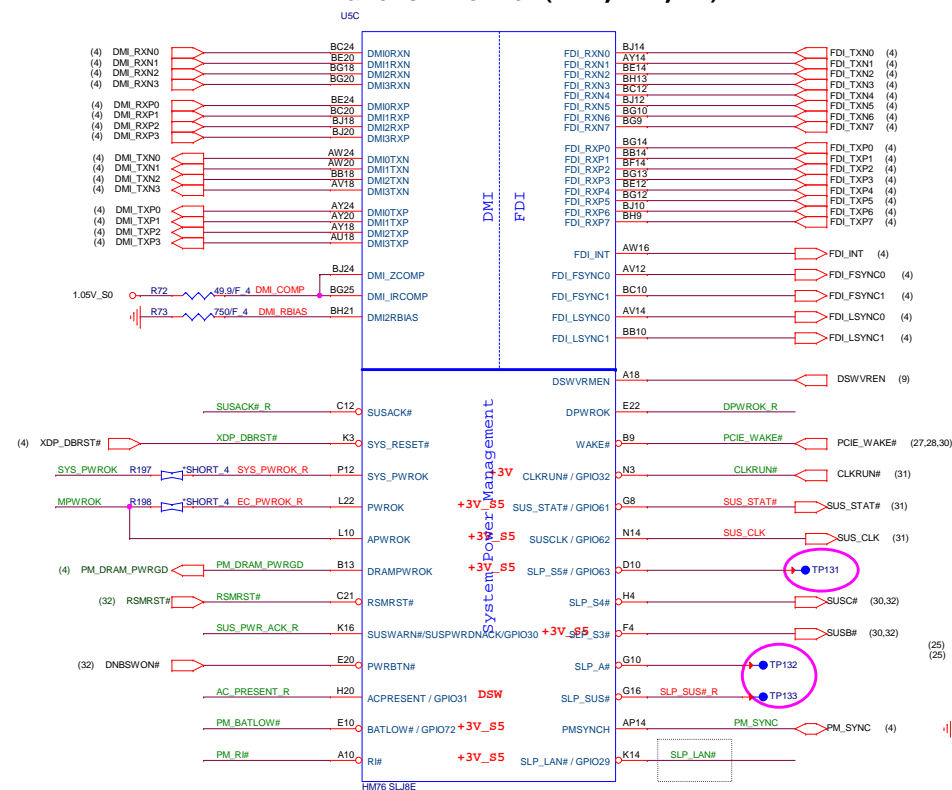


Processor Strapping

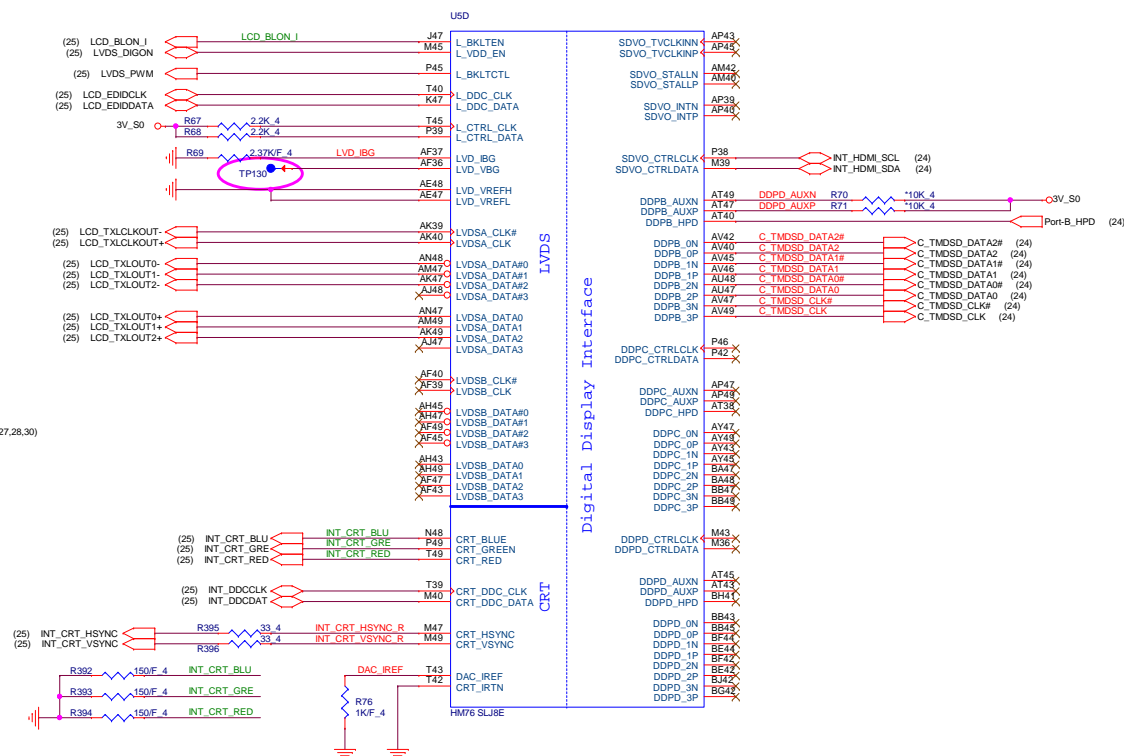
CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#



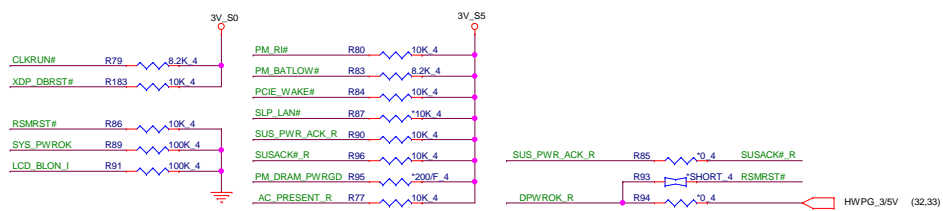
Panther Point (DMI,FDI,PM)



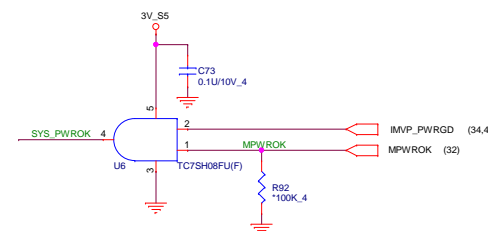
Panther Point (LVDS,DDI)



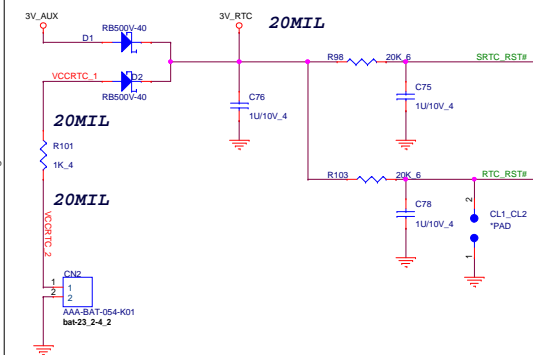
PCH Pull-high/low



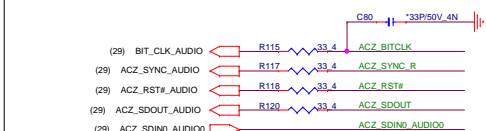
System PWR_OK



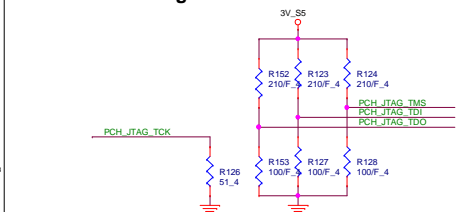
RTC Circuit



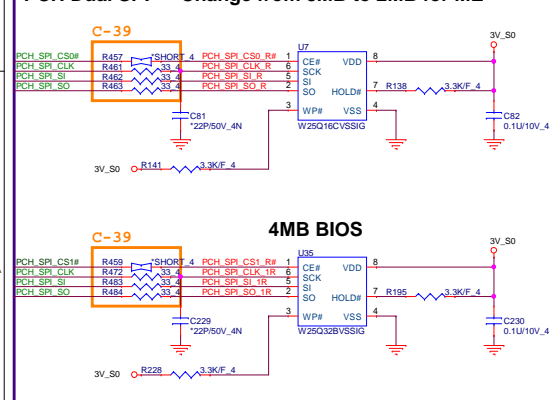
HDA Bus



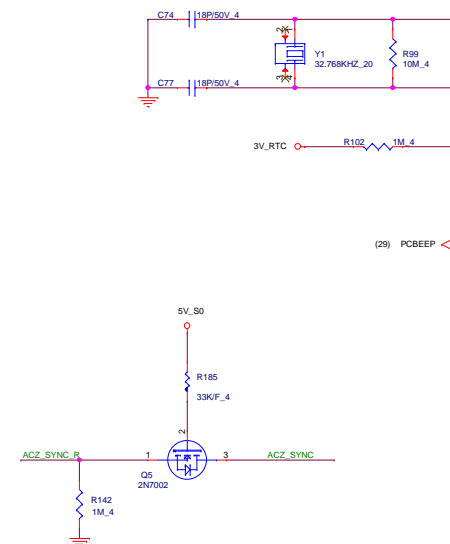
PCH JTAG Debug



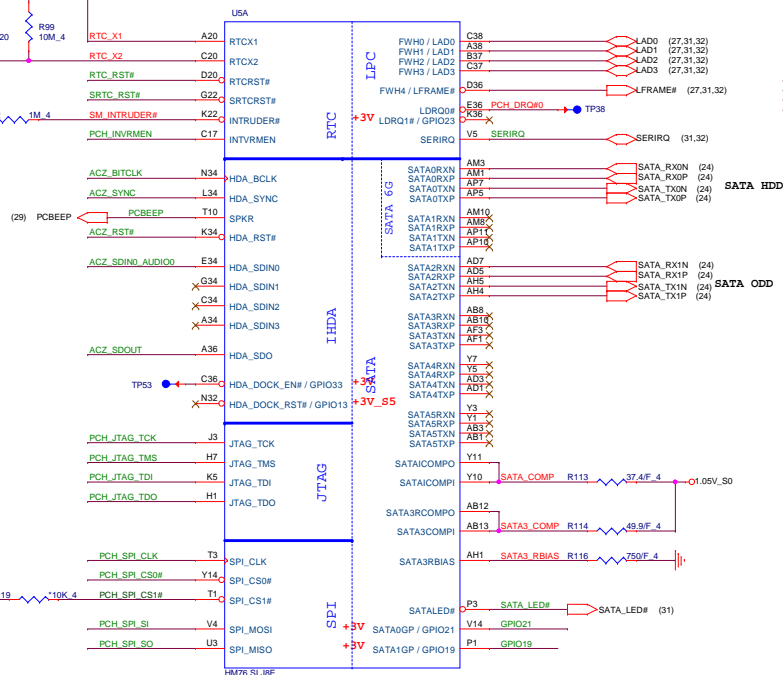
PCH Dual SPI	Change from 8MB to 2MB for ME
--------------	-------------------------------








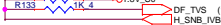




PCH2



Panther Point (HDA,JTAG,SATA)

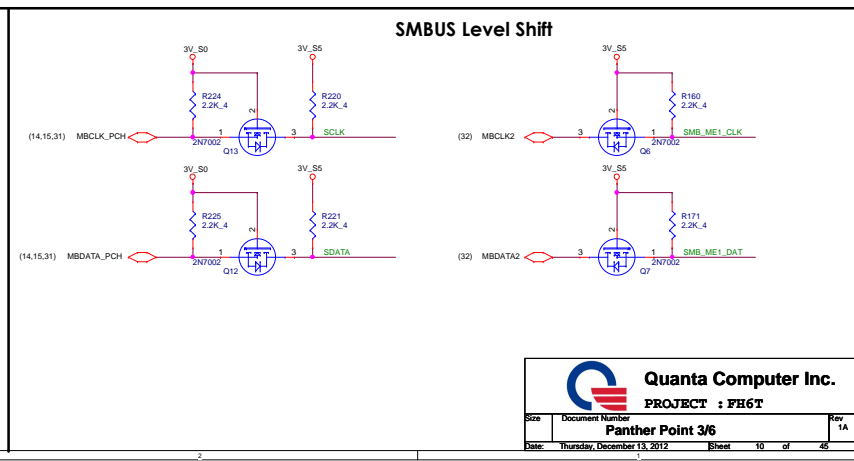
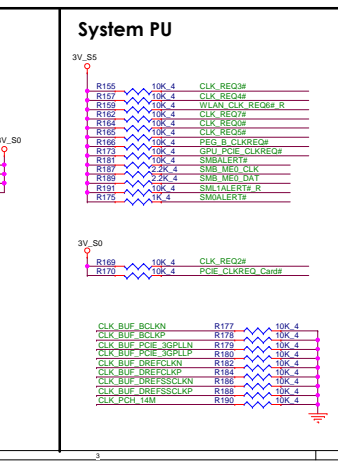
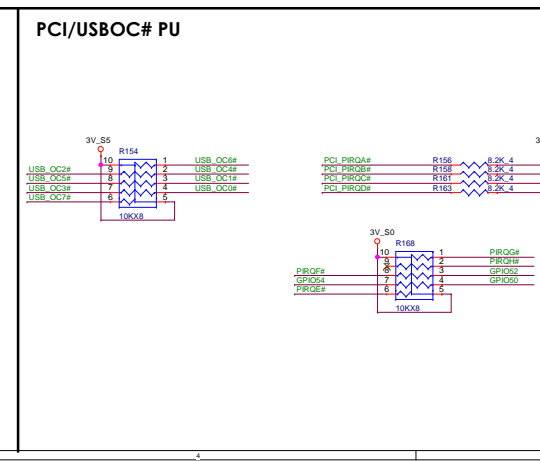
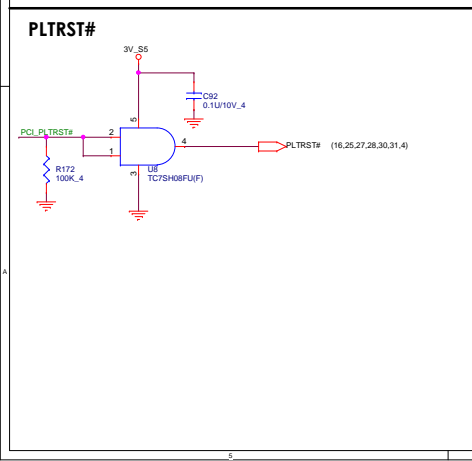
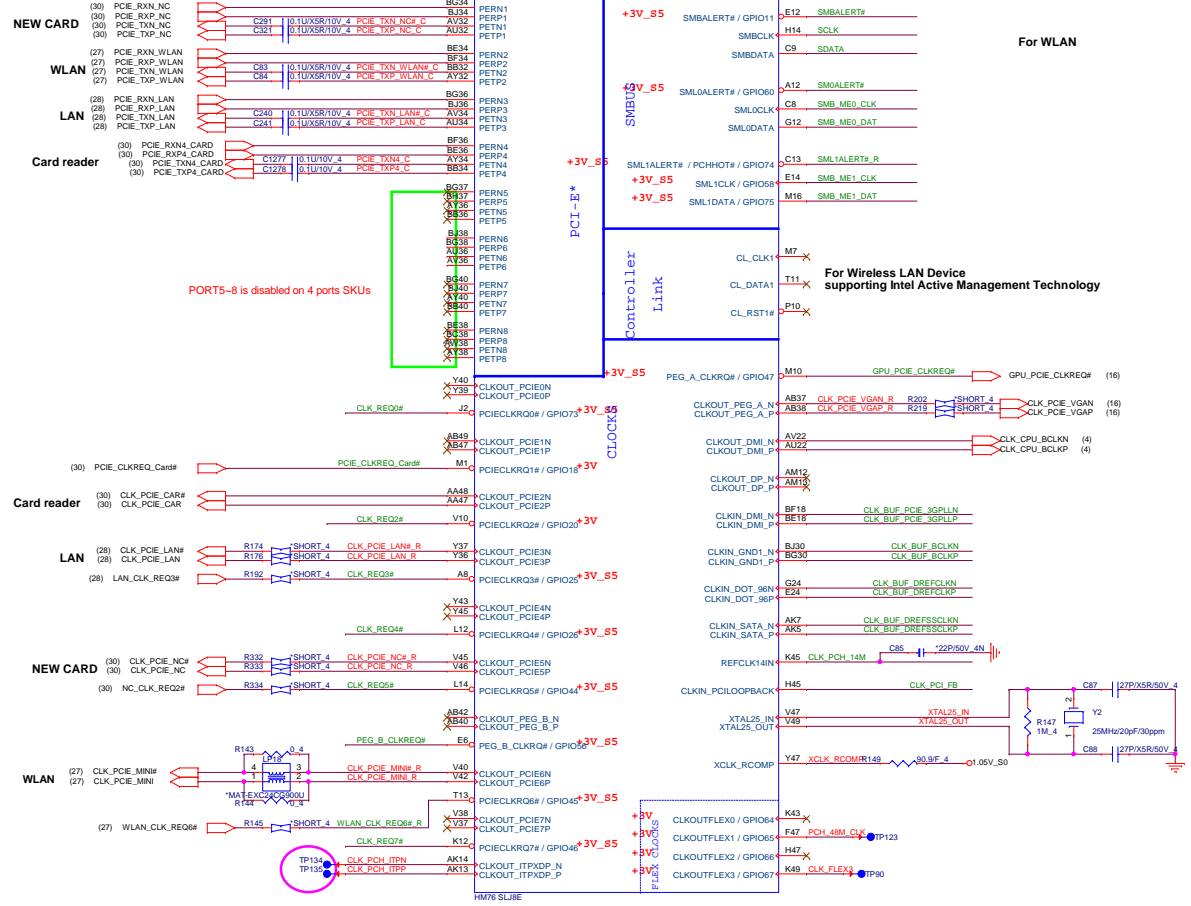
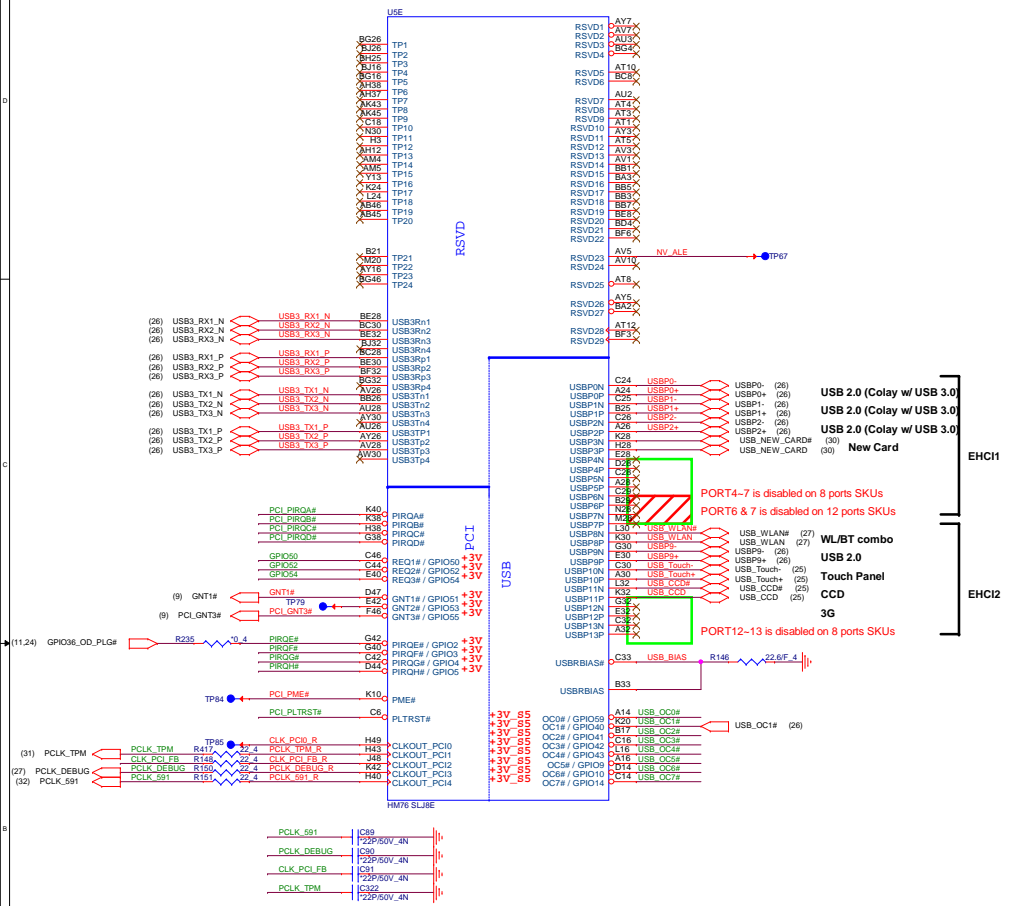


PCH Strap Table

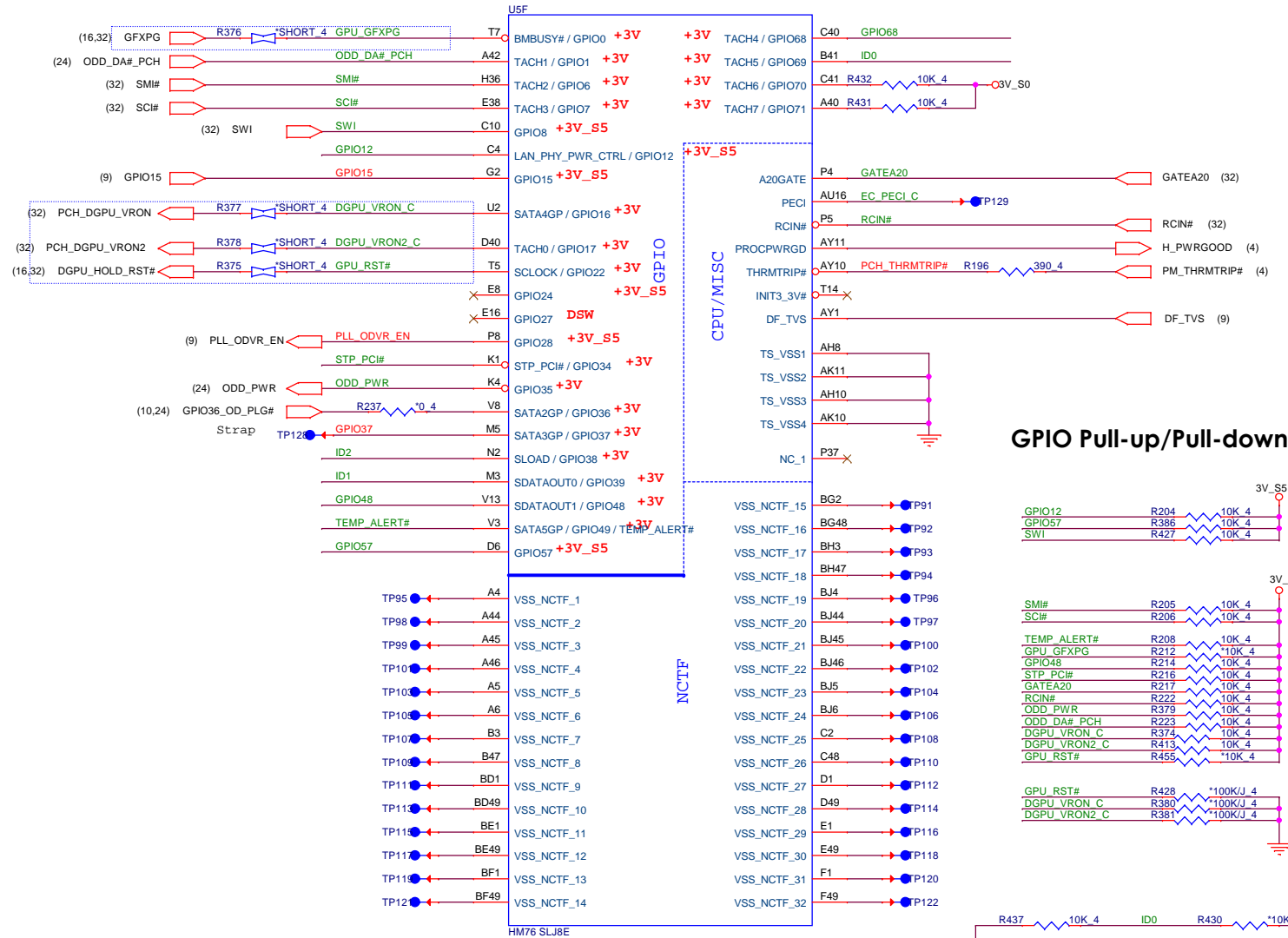
Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0  PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	 PCL_GNT3# (10)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC 									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"><thead><tr><th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr></thead><tbody><tr><td>1</td><td>1</td><td>SPI</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></tbody></table>	GNT1#	GPIO19	Boot Location	1	1	SPI	0	0	LPC	
GNT1#	GPIO19	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	1 = Override 0 = Default (weak PD 20K)	3V_S0 									
DF_TV5	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)										
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX 									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 									
GPIO15	TLS Confidentiality	RSMRST	0 = Default, TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	3V_RTC 									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT2# / GPIO53	ESi Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1= PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

Panther Point-M (PCI-E,SMBUS,CLK)

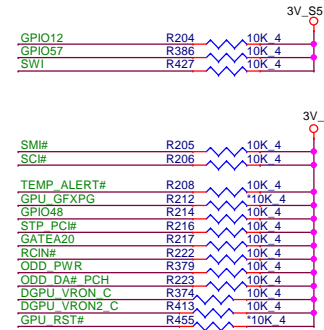
Panther Point-M (PCI,USB,NVRAM)




Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down



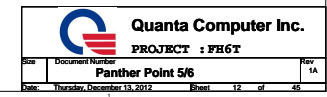
GPIO68	ID2	ID1	ID0	Model
1	0	0	0	FH6B UMA with click pad
1	0	0	1	
1	0	1	0	FH6 UMA(Consumer)
1	0	1	1	FH6 UMA(Commercial)
1	1	0	0	FH6 N13P-LP
1	1	0	1	FH6 N13P-GLP
1	1	1	0	TBD
1	1	1	1	TBD
0	0	1	0	FH6T UMA
0				
0				

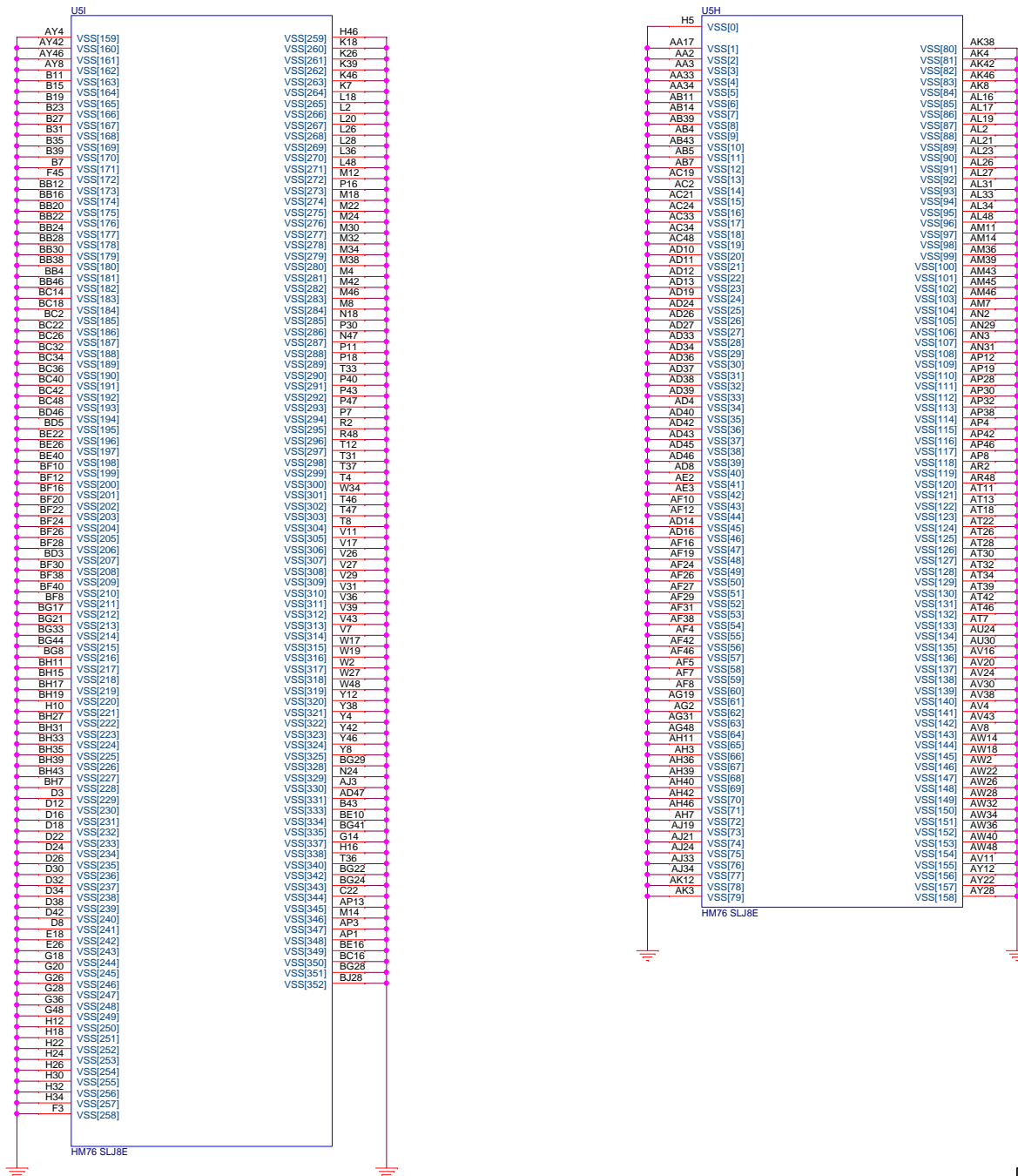


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PROJECT : FH6T

Size	Document Number	Rev 1A
Panther Point 4/6		
Date:	Thursday, December 13, 2012	Sheet 11 of 45

Panther Point-M (POWER)



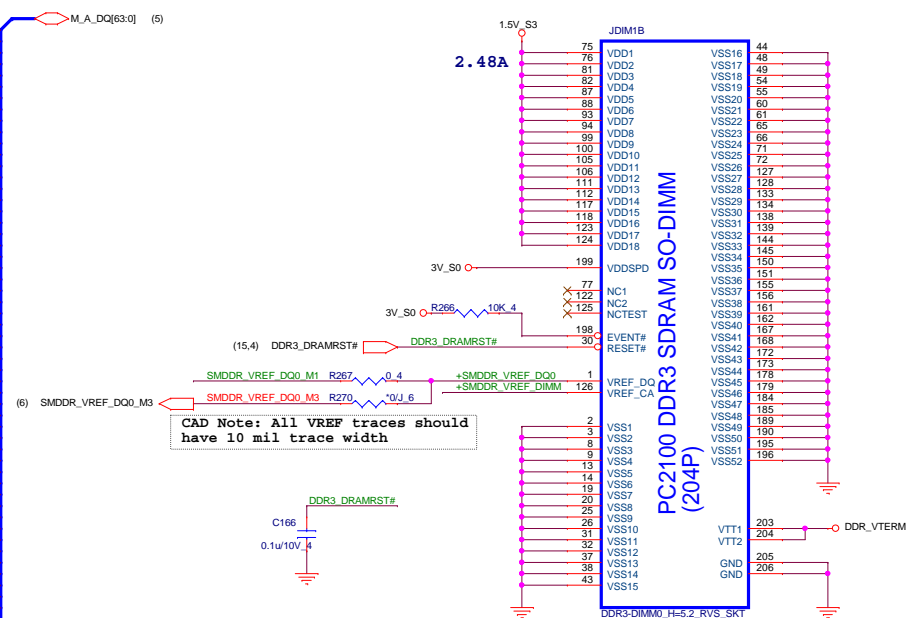
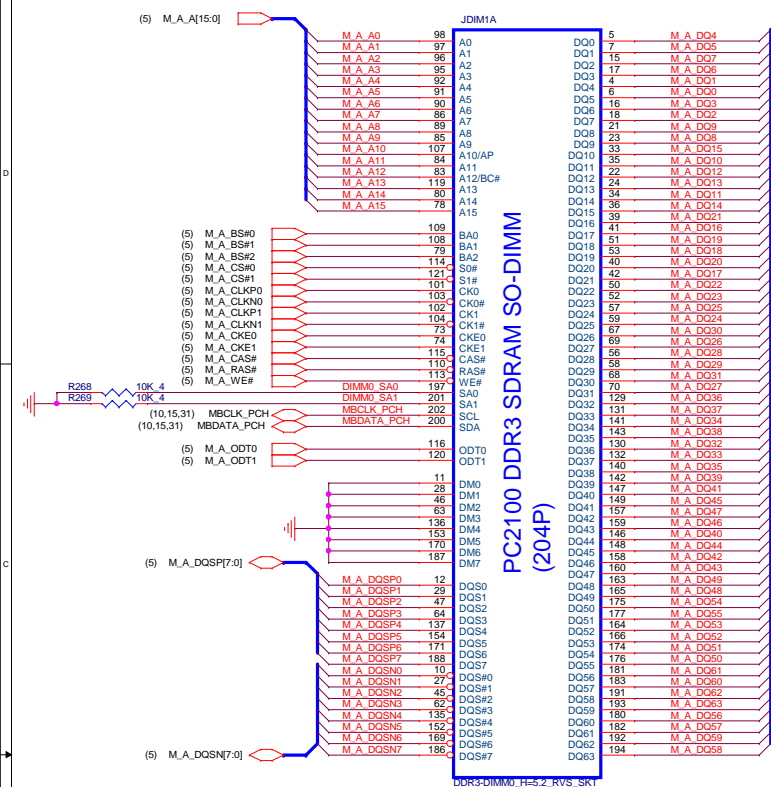


Quanta Computer Inc.

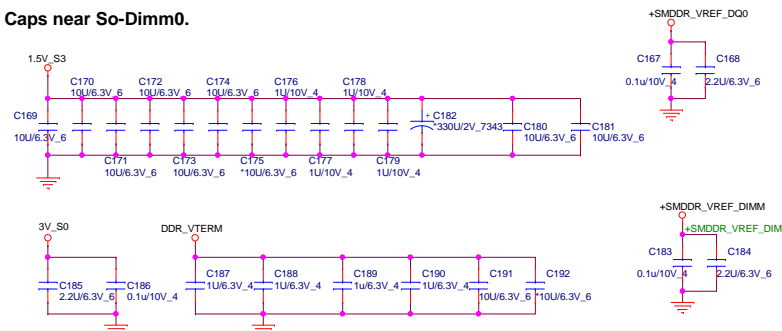
PROJECT : FH6T

Size	Document Number	Rev
	Panther Point 6/6	1A
Date:	Thursday, December 13, 2012	Sheet 13 of 45

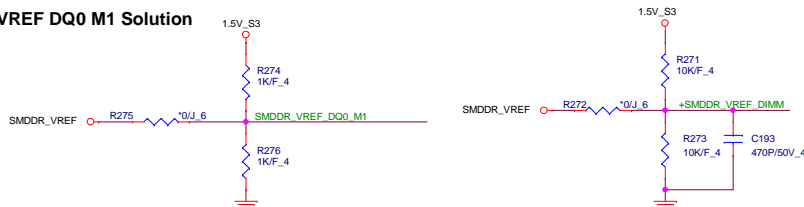
DDR_STD(DDR)



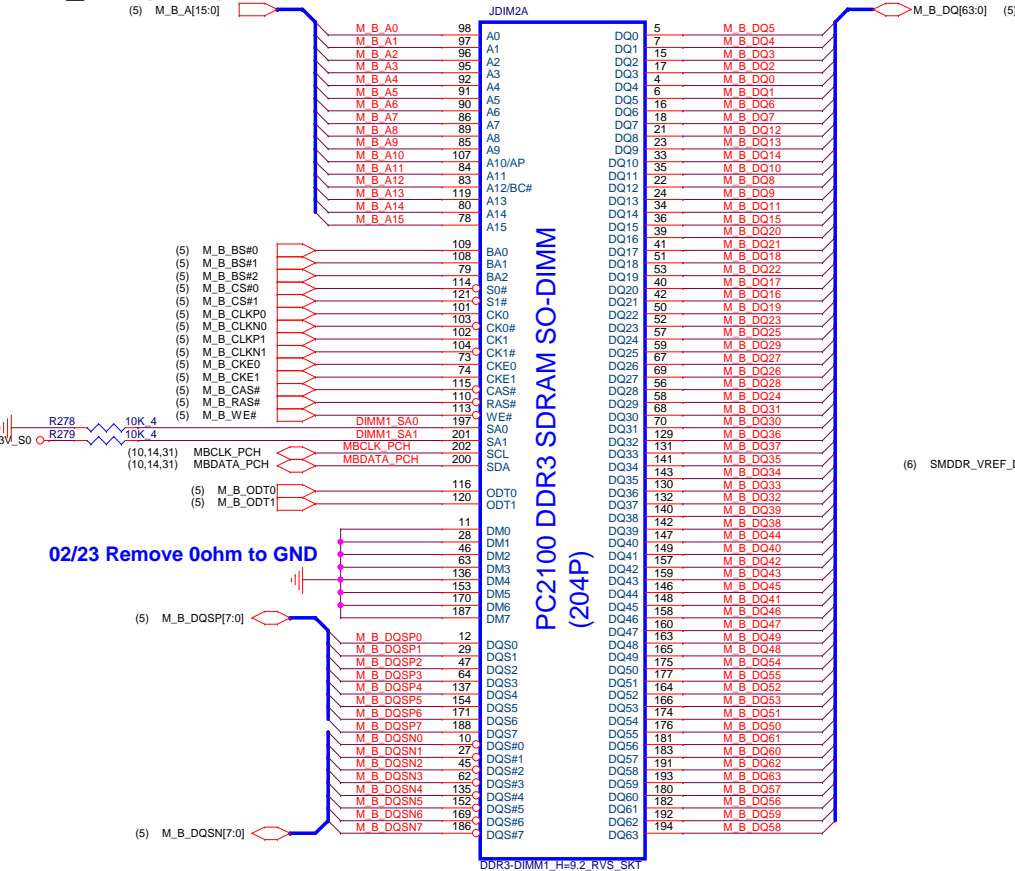
Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



DDR_RVS (DDR)

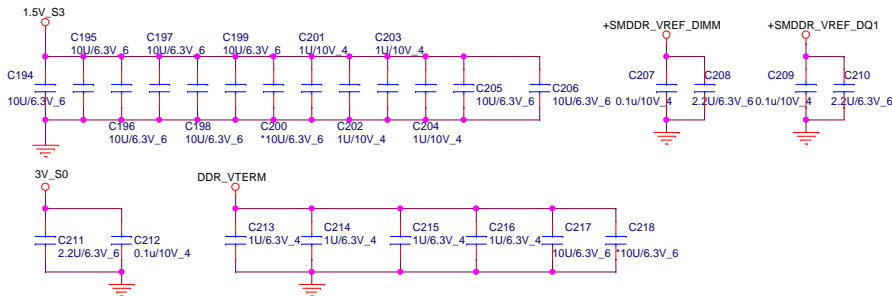


02/23 Remove 0ohm to GND

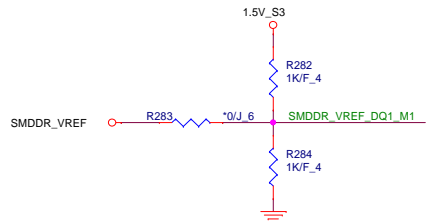
PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=9.2_RVS_SK1

Place these Caps near So-Dimm1.



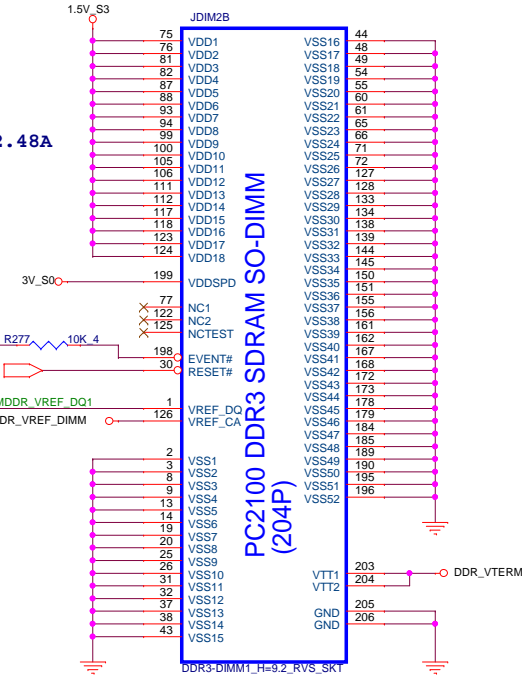
VREF DQ1 M1 Solution



2.48A

(6) SMDR_VREF_DQ1_M3

CAD Note: All VREF traces should have 10 mil trace width



PC2100 DDR3 SDRAM SO-DIMM (204P)

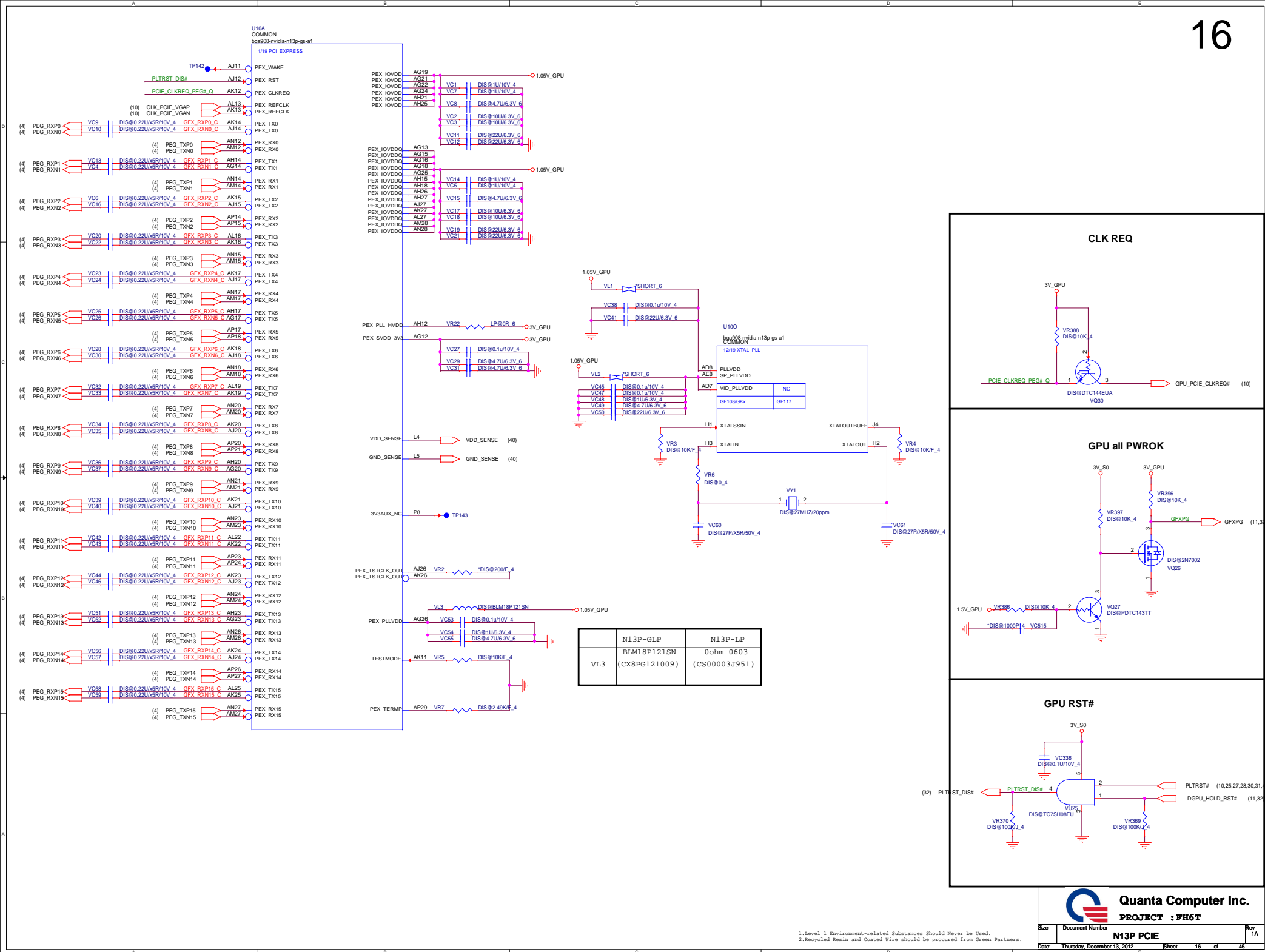
DDR3-DIMM1_H=9.2_RVS_SK1

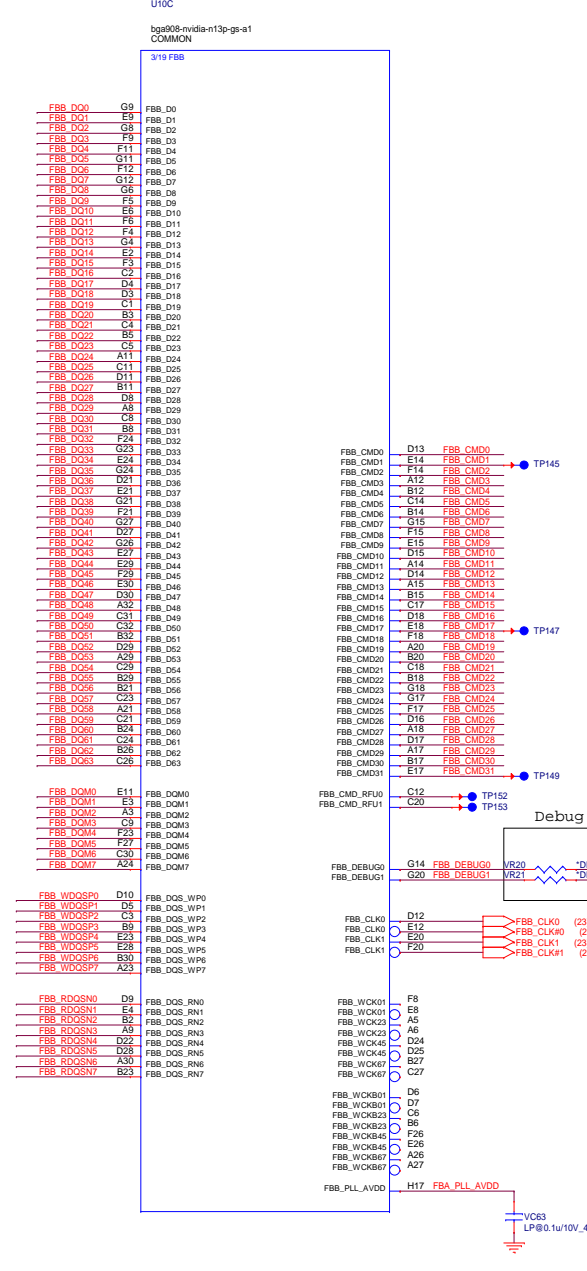


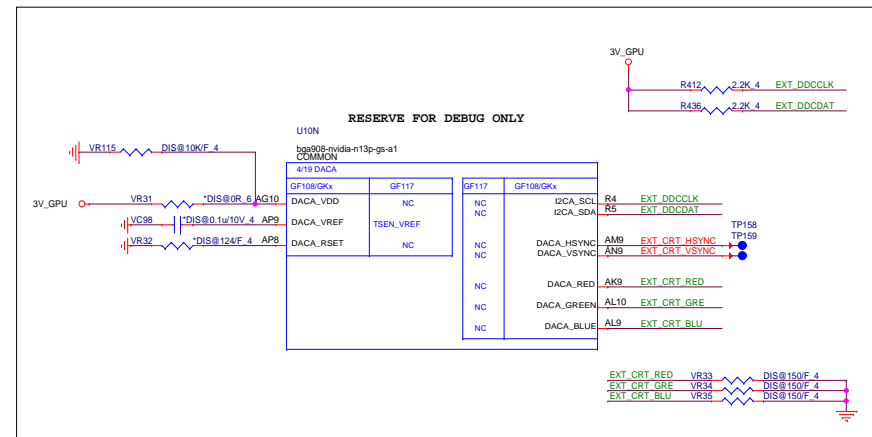
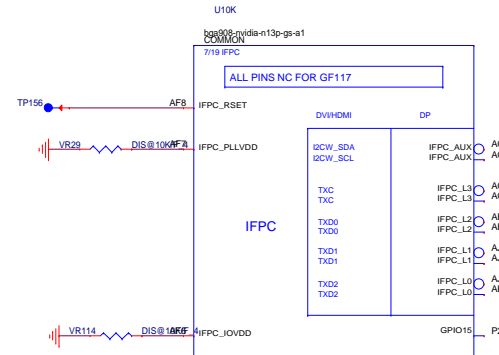
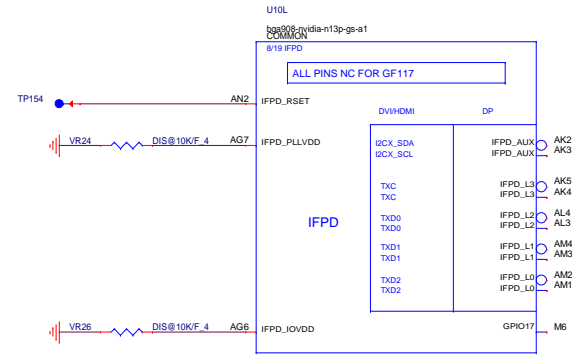
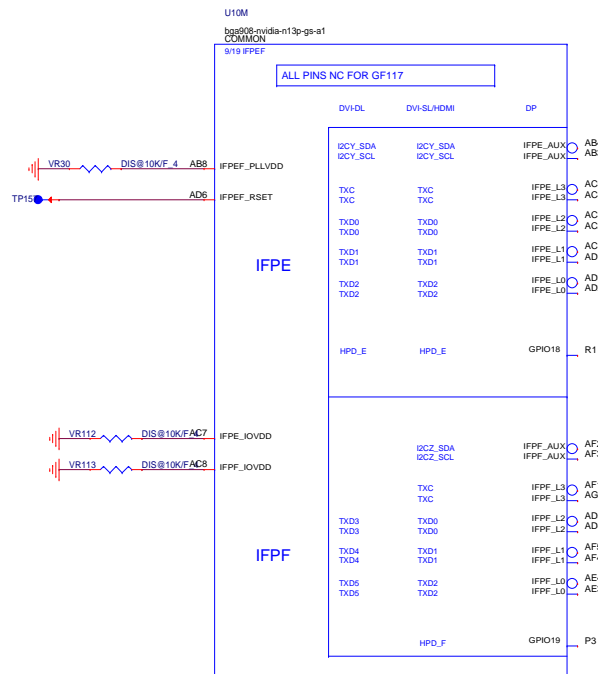
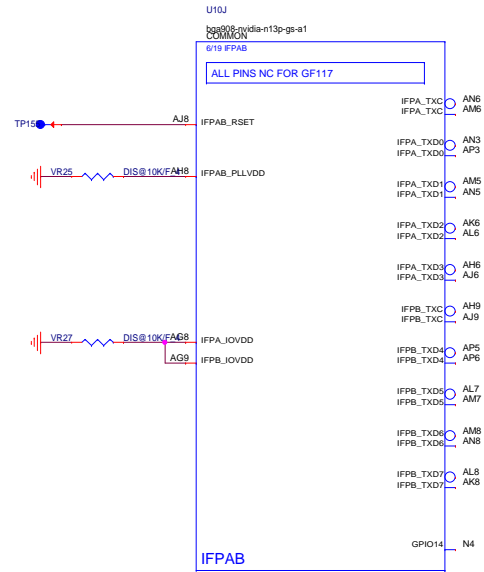
Quanta Computer Inc.

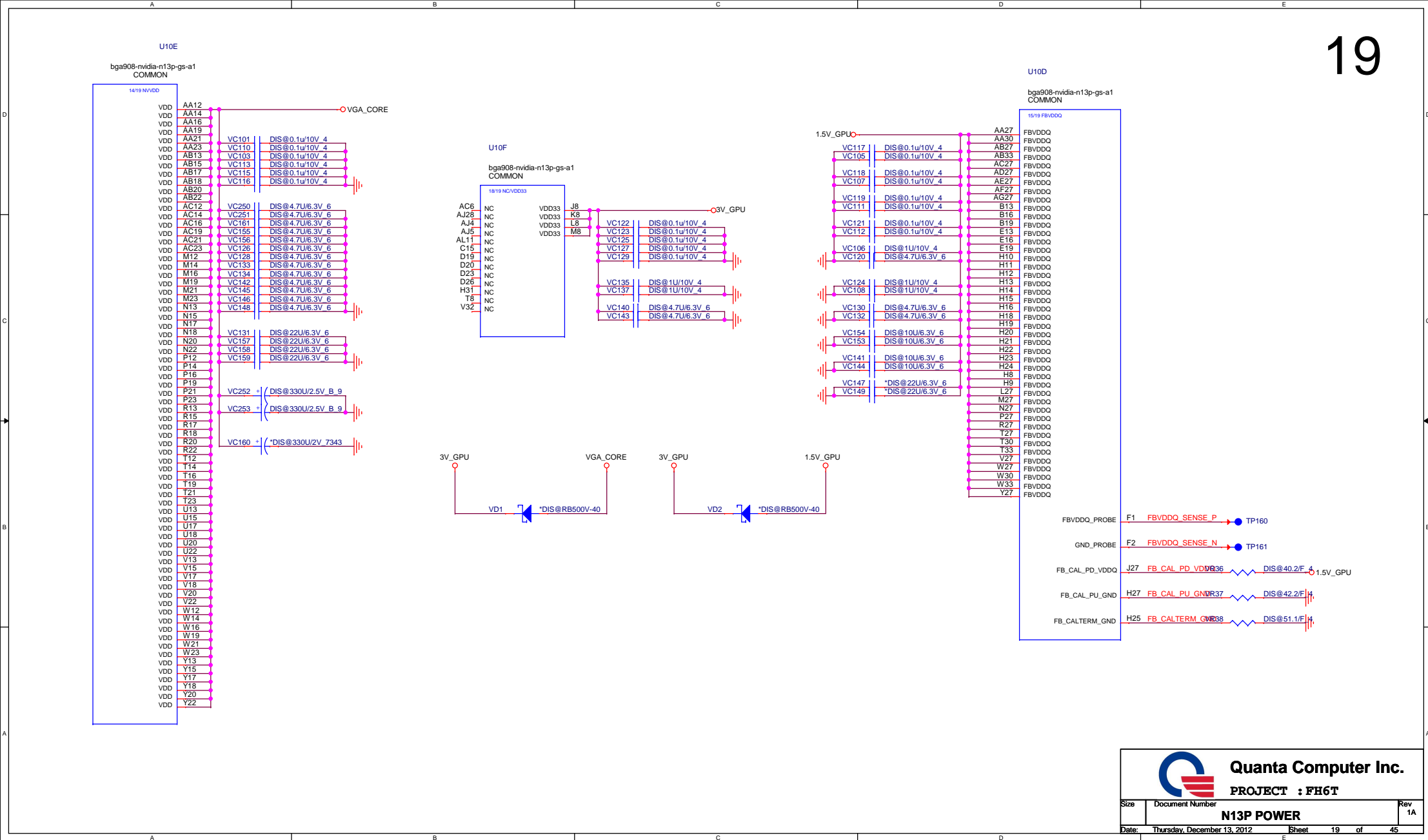
PROJECT : FH6T

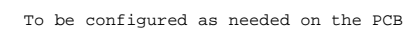
Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date:	Thursday, December 13, 2012	Sheet 15 of 45

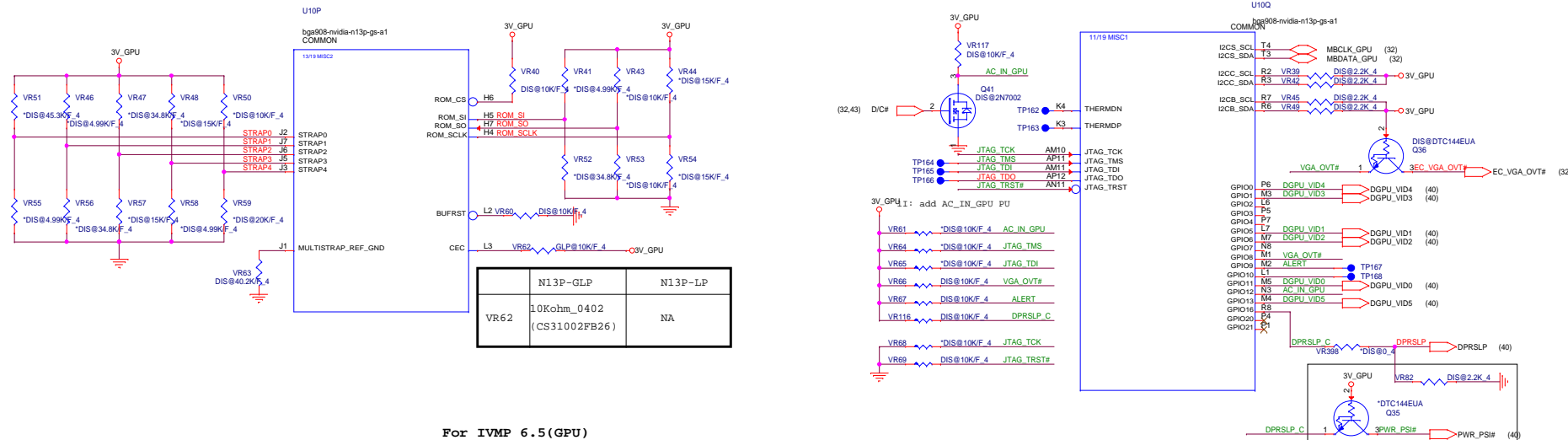










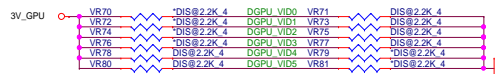


For IVMP 6.5 (GPU)

Logical Strap Bit Mapping

Value	PU-VDD	PD	QCI PN(0402)
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS3482FB22
45.3K	1111	0111	CS35432FB18

Default:0.9V (0110000) N13P-GLP/LP
Note:VID6 PD in VR Side



VRAM(DDR3) Configuration Table

RAMCFG [3:0]	DESCRIPTION (Vendor P/N)	Vendor	QCI P/N	ROM_S
0111	128*16-900MHz K4W2G1646C-HC11	Samsung	AKD5MGWT500	PD 45.3K
0110	128*16-900MHz H5TQ2G63BFR-11C	Hynix	AKD5MGWTW00	PD 35K
0010	64*16-900MHz H5TQ1G63DFR-11C	Hynix	AKD5LZWTW02	PD 15K
0011	64*16-900MHz K4W1G1646G-BC11	Samsung	AKD5EGGT500	PD 20K

N13P-LP (GK107-ESP)	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG-6LP PCI_DEVIDE[5]-LP	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	XCLK_417 FB[1]-LP	FB_0_BAR_SIZE FB[0]-LP	SMB_ALT_ADDR I2CS ADDR:0X9E	VGA_DEVICE
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	Reserve PCIE_SPEED-LP	PCIE_MAX_SPEED	DP_PLL_VDD3V

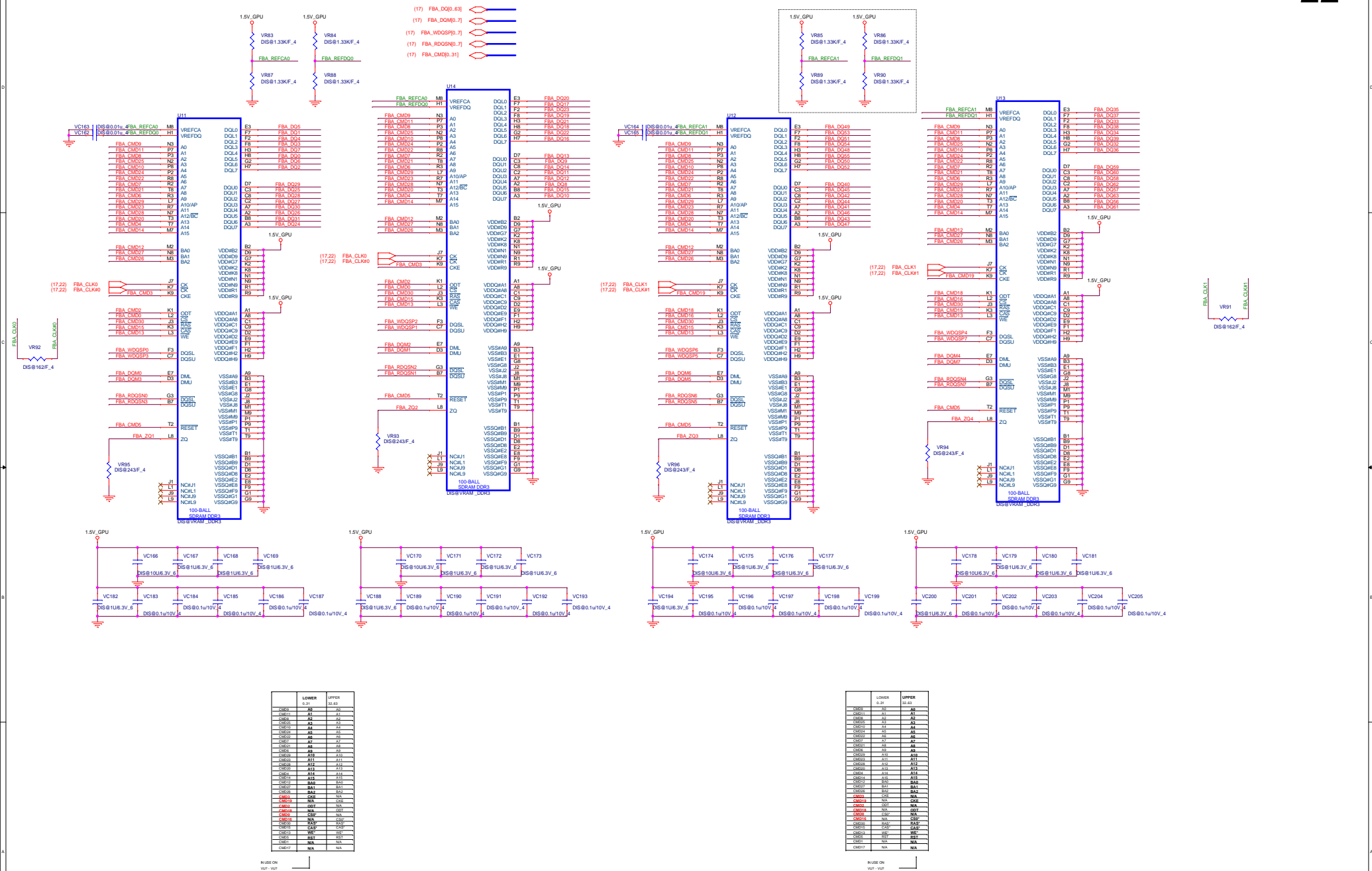
B-29

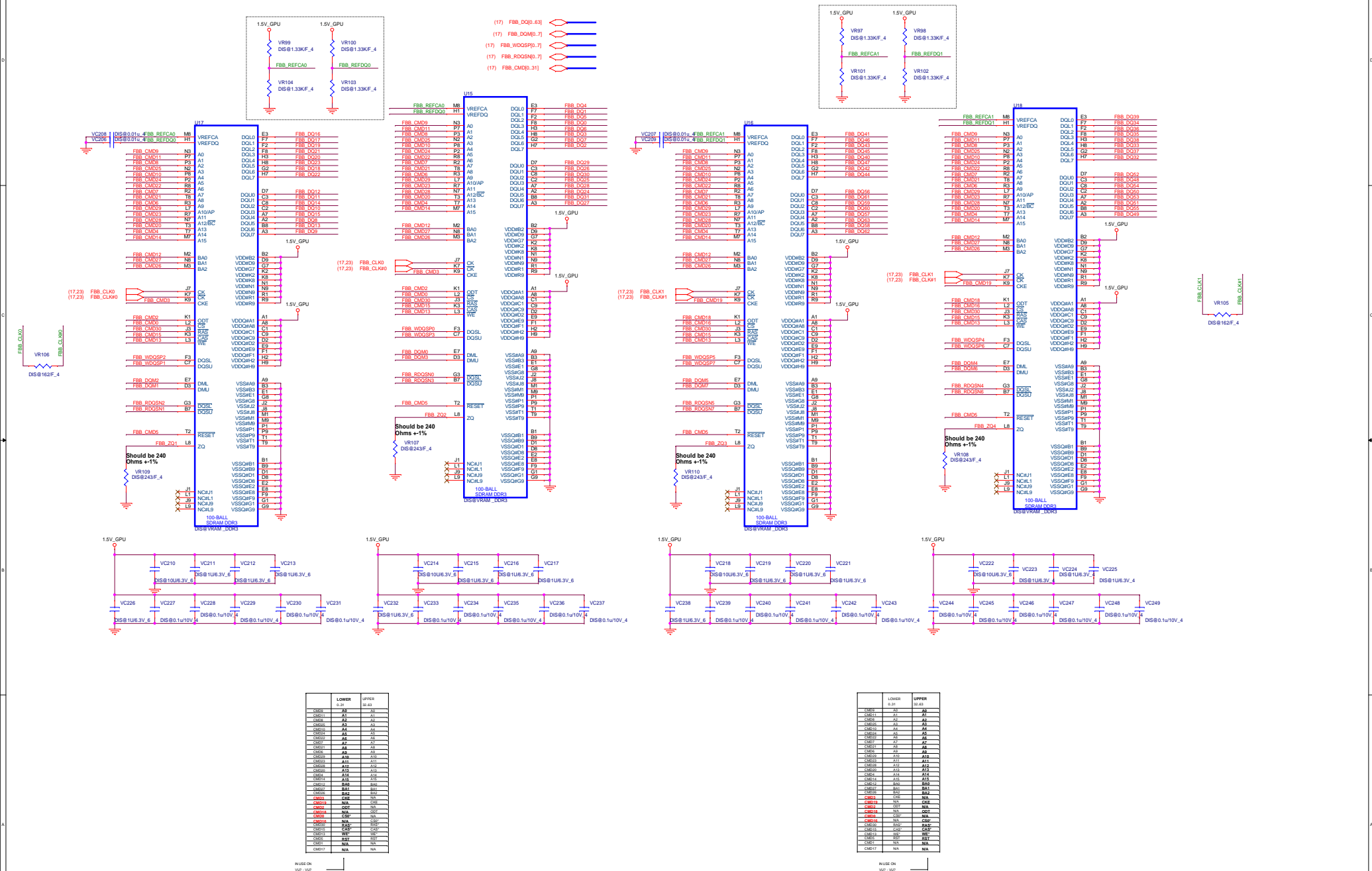
		GLP 1GB HYN	GLP 1GB SAM	GLP 2GB HYN	GLP 2GB SAM	LP 2GB HYN	LP 2GB SAM
ROM_SCLK	VR44 VR54	NA CS31502FB24	NA CS31502FB24	CS31502FB24	NA CS31502FB24	CS24992FB26 NA	CS24992FB26 NA
ROM_SI	VR41 VR52	NA CS31502FB24	NA CS32002FB29	CS33012FB18	CS34532FB18	NA CS33012FB18	NA CS34532FB18
ROM_SO	VR43 VR53	NA CS31002FB26	NA CS31002FB26	CS31002FB26	CS31002FB26	CS31002FB26 NA	CS31002FB26 NA
STRAP0	VR51 VR55	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA	CS34532FB18 NA
STRAP1	VR46 VR56	NA CS34532FB18	NA CS34532FB18	CS34532FB18	CS34532FB18	NA CS24992FB26	NA CS24992FB26
STRAP2	VR47 VR57	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	NA CS32002FB29	NA CS32002FB29
STRAP3	VR48 VR58	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA	CS24992FB26 NA
STRAP4	VR50 VR59	NA NA	NA NA	NA NA	NA NA	NA CS34532FB18	NA CS34532FB18

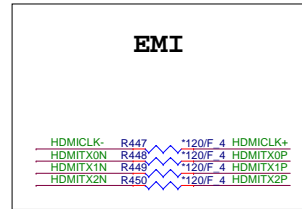
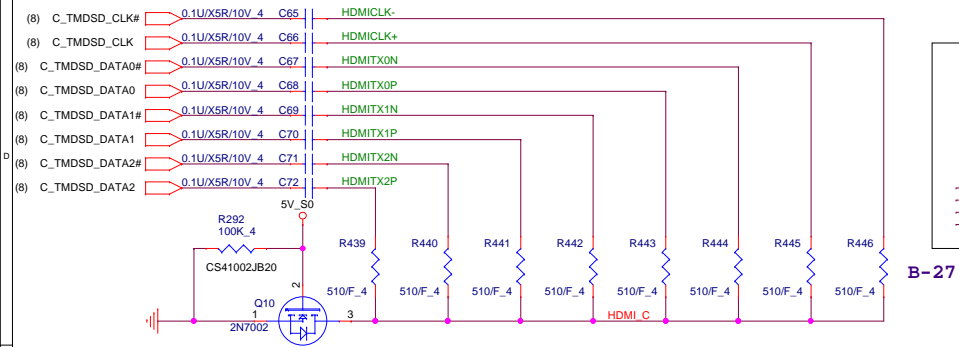
Value	Note	
1000	LP:ES Samples 5K PU(0X0FDB)	*LP QS Samples:5K PU(0X0FD3)
0010	GLP: ES Samples 15K PD(0X0DFE)	*GLP MP Samples 15K PD(0X0DE8)
0110	LP H5T0G63BFR-11C 35K PD	*H5TQ2G63DFR-11C: 30.1K PD(0X5)
0100	K4W2G1646G-BC11 45.3K PD	
0010	H5T0G1663DFR-11C 15K PD	
0011	GLP K4W1G1646G-BC11 20K PD	
1001	10K PU	
0001	10K PD	
1111	EDID is used :45K PU	
0000	LP:notebook default:35K PD	*LP QS Samples: 4.99K PD(0X0)
0111	GLP: Reserve:45.3K PD	
0011	LP ES Samples:20K PU(0X0FDB)	*LP QS Samples: 20K PD(0X0FD3)
1000	GLP ES Samples:45.3K PU(0X0DEF)	*GLP MP Samples: 5K PU(0X0DE8)
0000	Not in use :5K PD	
0111	LP:10K PD GLP: NA	*LP QS Samples: 45K PD(0X111)

GPIO ASSIGNMENTS

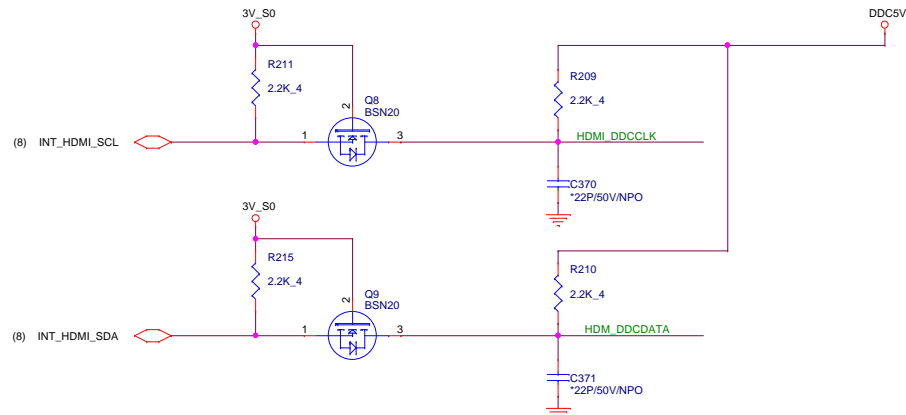
GPIO	I/O	USAGE	
0	OUT	Y	NVDD VID4
1	OUT	Y	NVDD VID3
2	OUT	N	PANEL BACKLIGHT PWM
3	OUT	N	PANEL POWER ENABLE
4	OUT	N	PANEL BACKLIGHT ENABLE
5	OUT	Y	NVDD VID1
6	OUT	Y	NVDD VID2
7	OUT	N	3D STEREO
8	I/O	Y	GPU Overtemp
9	I/O	Y	GPU ALERT
10	OUT	N	FB Vref Control
11	OUT	Y	NVDD VID0
12	IN	N	PWR_Level AC Detect
13	OUT	Y	NVDD VID5
14	IN	N	HPD for IFP AB
15	IN	N	HPD for IFP C
16	OUT	N	DPRSLP(Default) or PSI#
17	OUT	N	HPD for IFP D
18	OUT	N	HPD for IFP E
19	OUT	N	HPD for IFP F
20	OUT	N	
21	OUT	N	



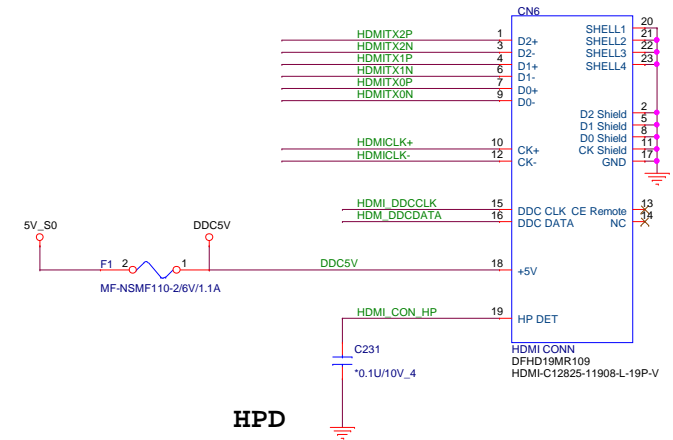




DDC Level Shift

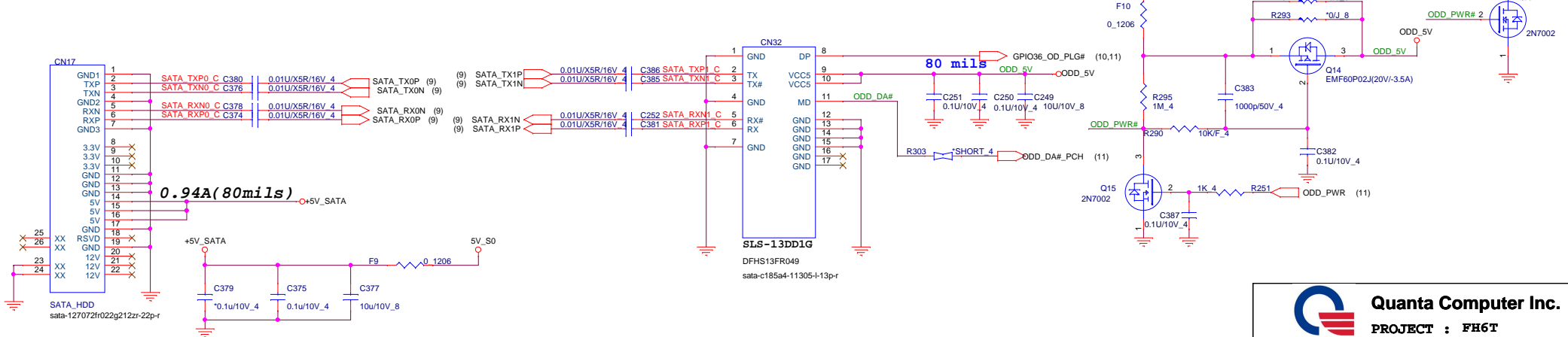


HDMI Conn

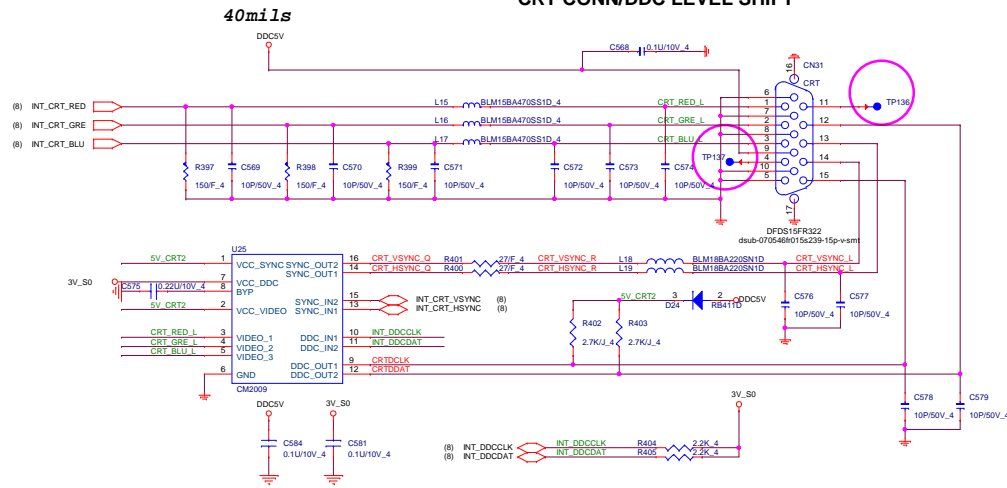


SATA ODD

2.5" SATA HDD

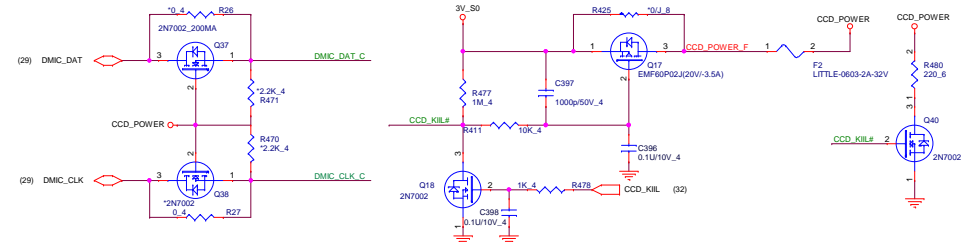


CRT CONN/DDC LEVEL SHIFT

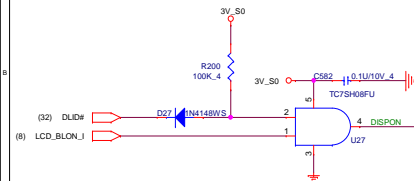


C-37

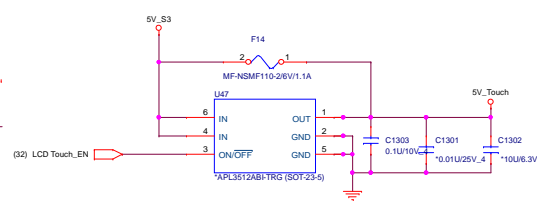
CCD KILL



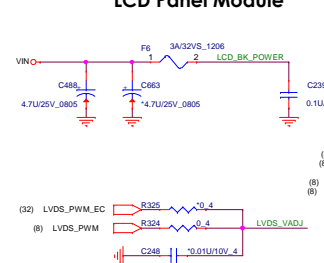
PANEL BACKLIGHT CONTROL



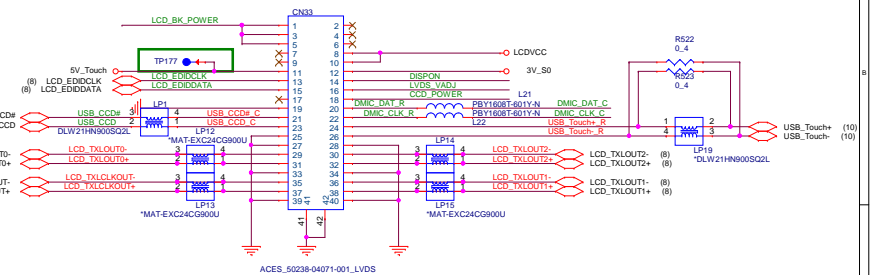
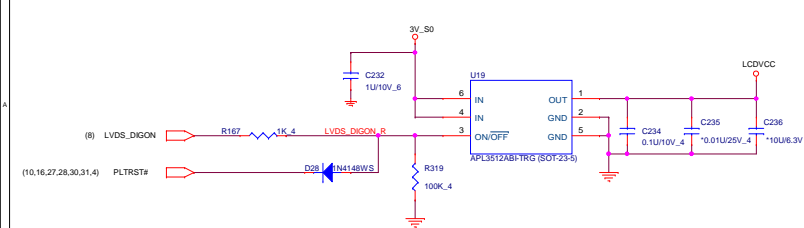
Touch Panel POWER SWITCH



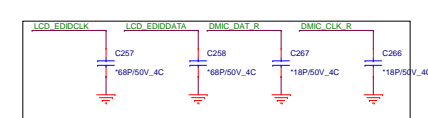
LCD Panel Module



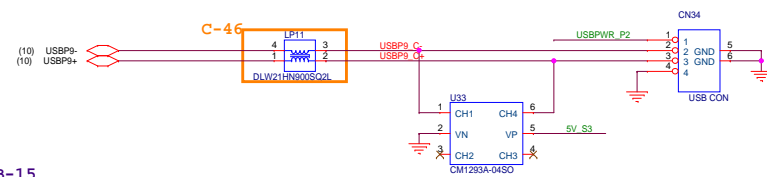
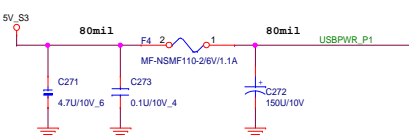
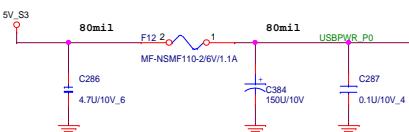
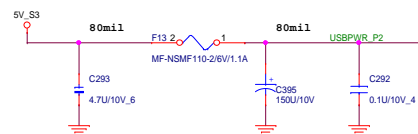
LCD POWER SWITCH



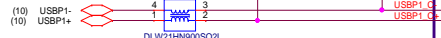
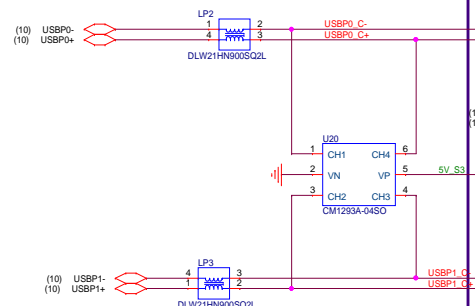
EMI



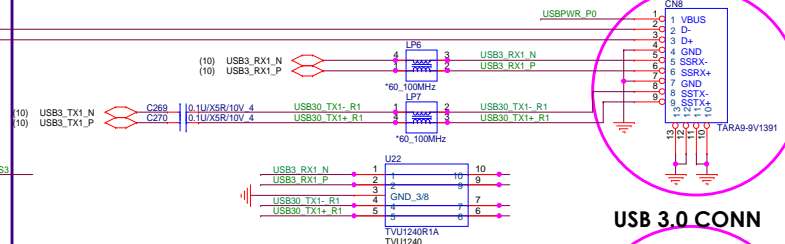
60mils



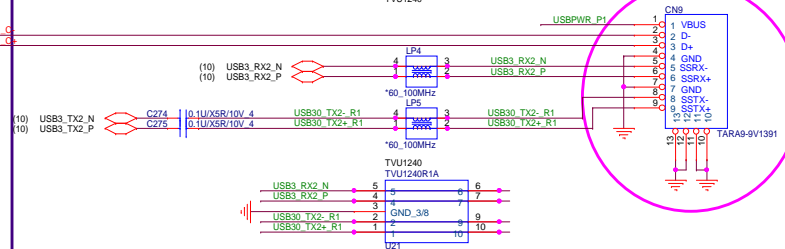
B-15



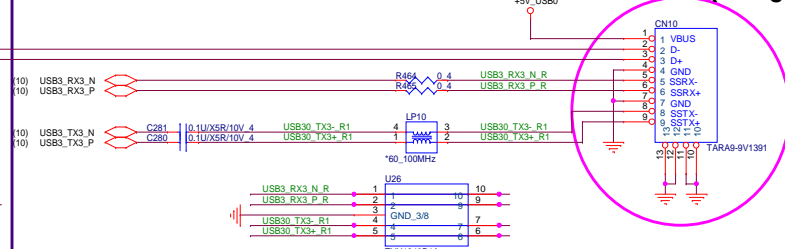
USB 3.0 CONN



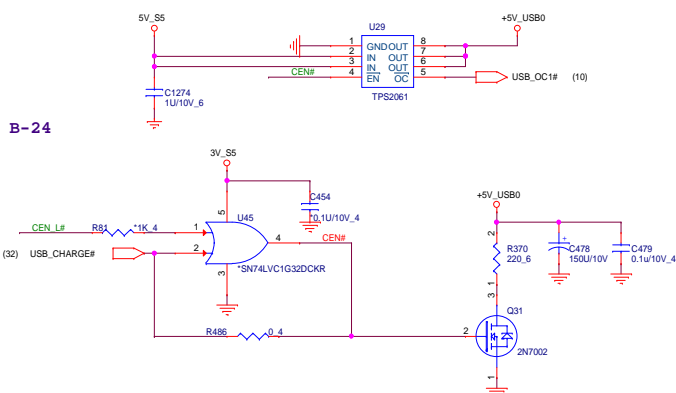
USB 3.0 CONN



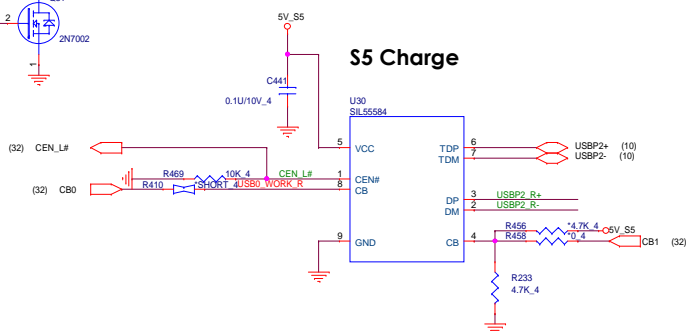
USB 3.0 CONN(Charge)



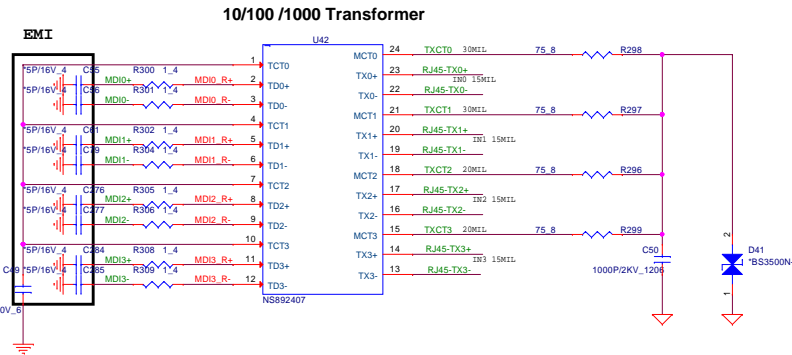
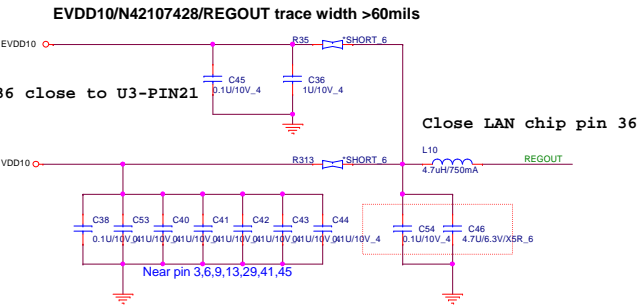
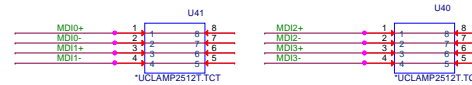
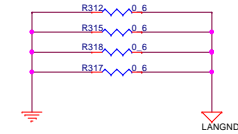
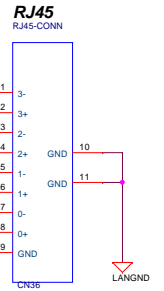
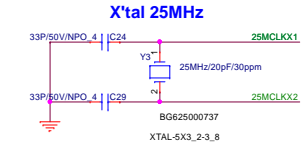
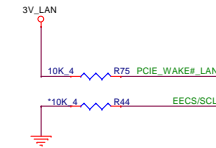
B-24

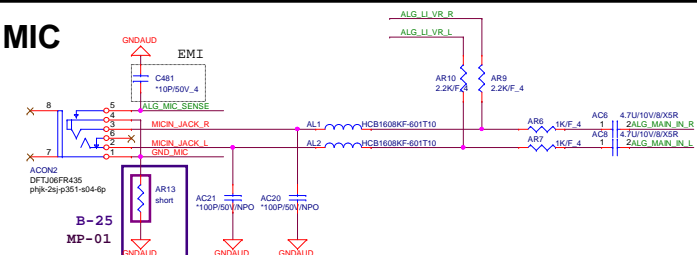


S5 Charge

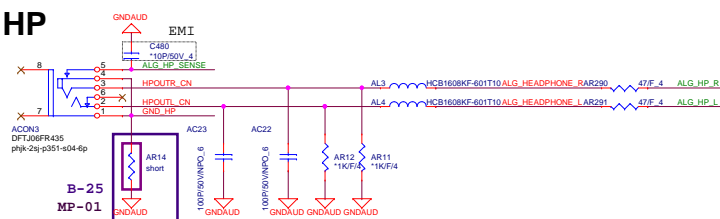


CB0	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG55584 only)

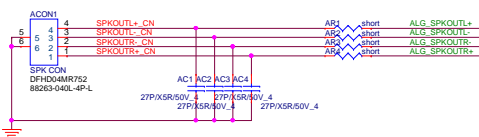




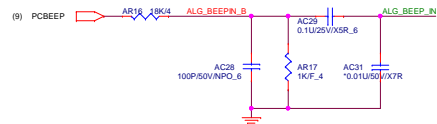
HP



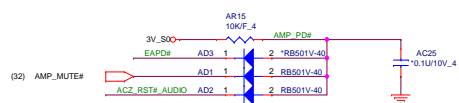
SPKR



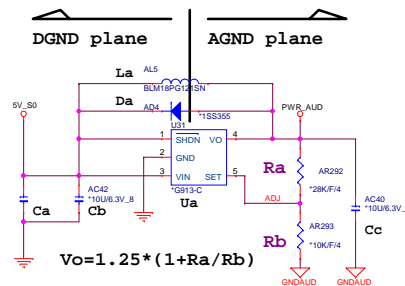
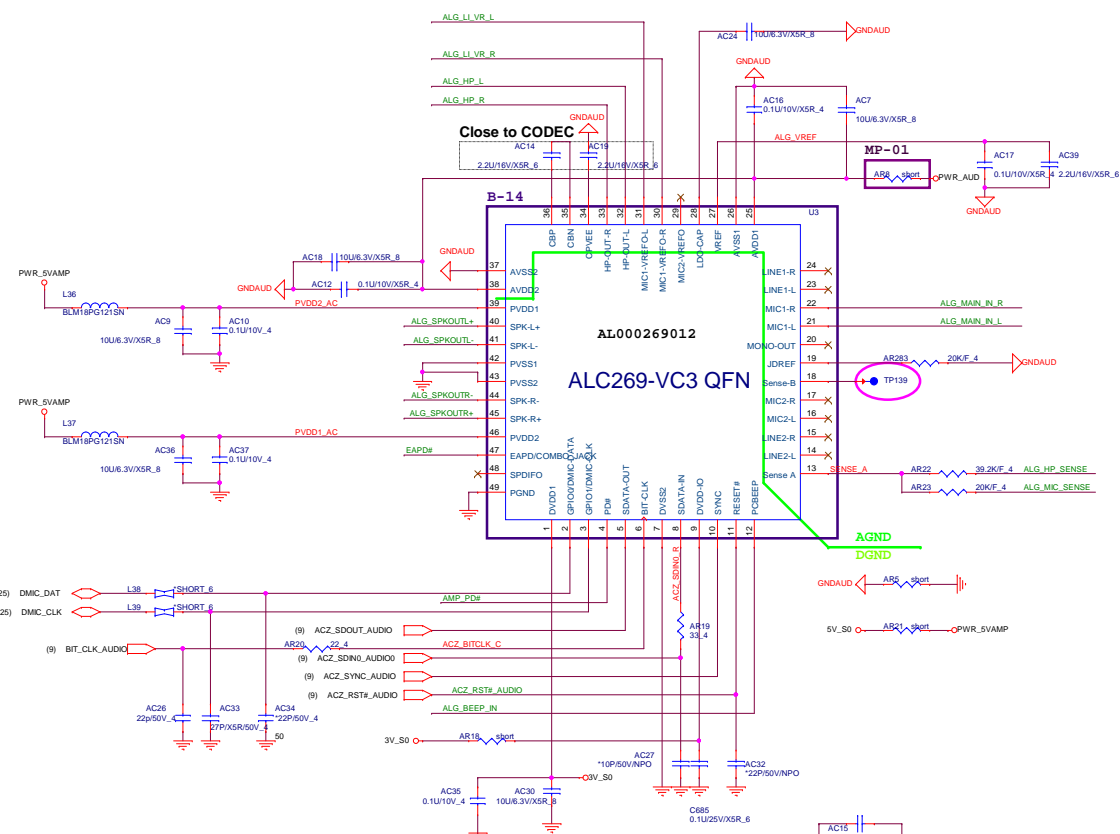
BEEP



VOLMUTE

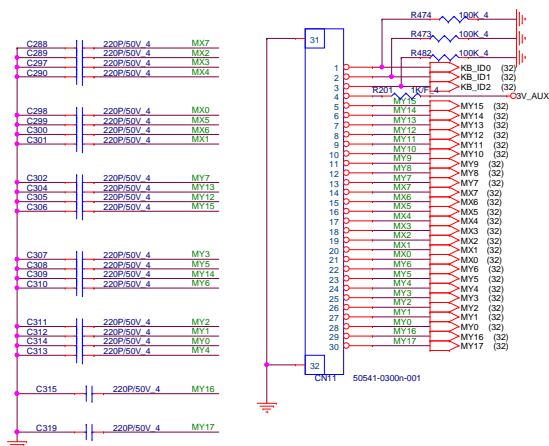


Codec ALC269-VC3



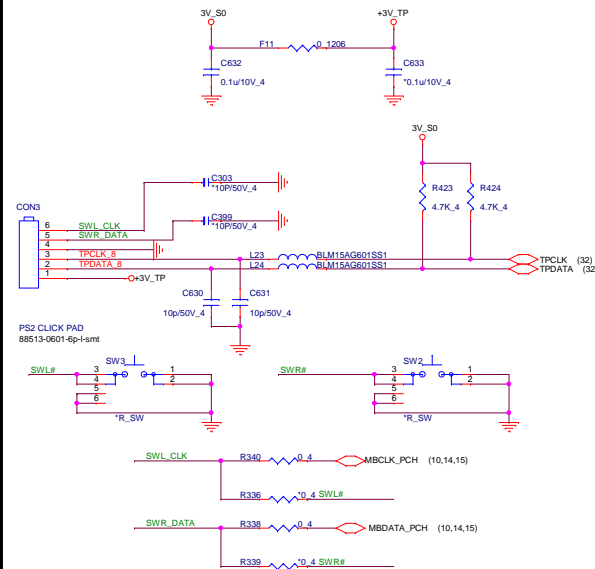


INT KeyBoard

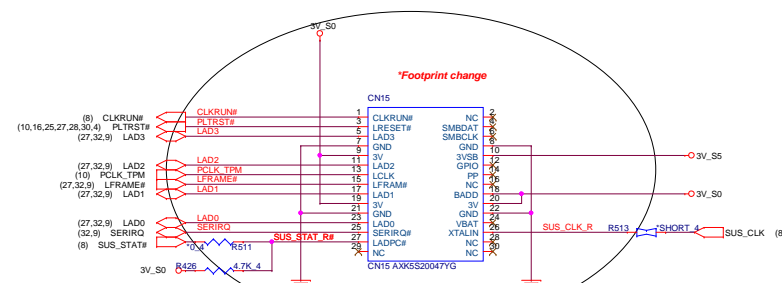


	ID0	ID1	ID2		KB_ID
			CHO	ISO	
UK	1	0	0	1	1
US	0	1	0	1	1
JP	1	1	0	1	1

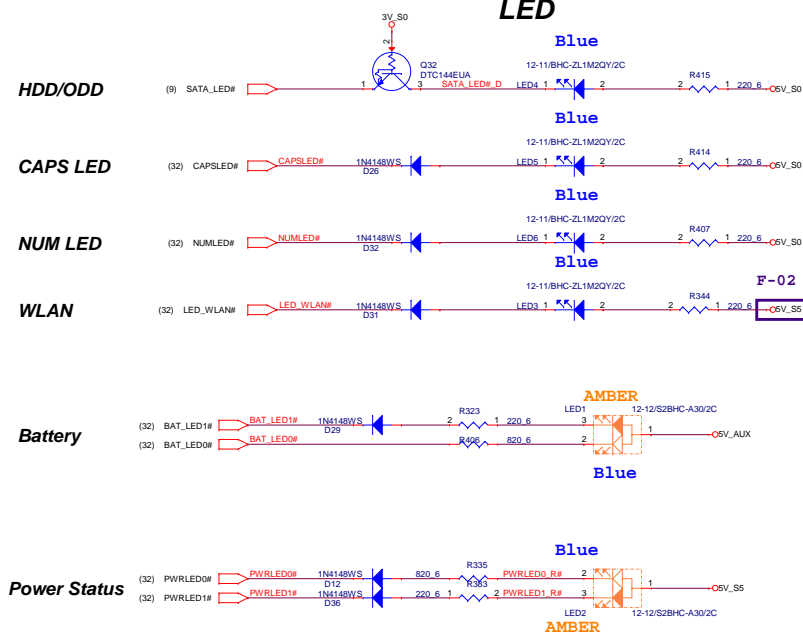
Touch Pad / Click PAD



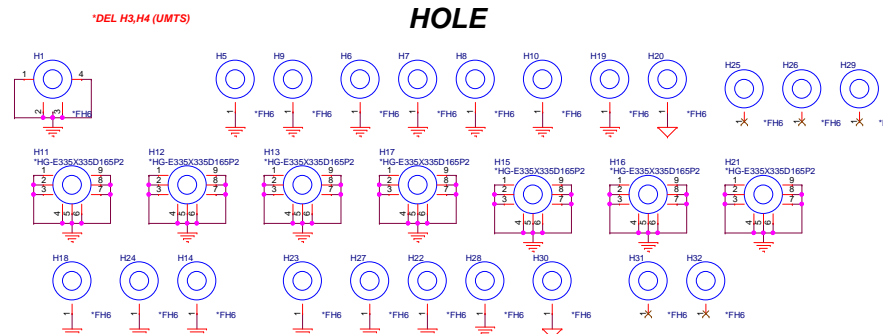
TPM Connector



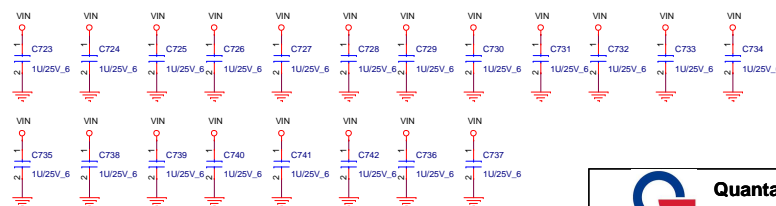
LED

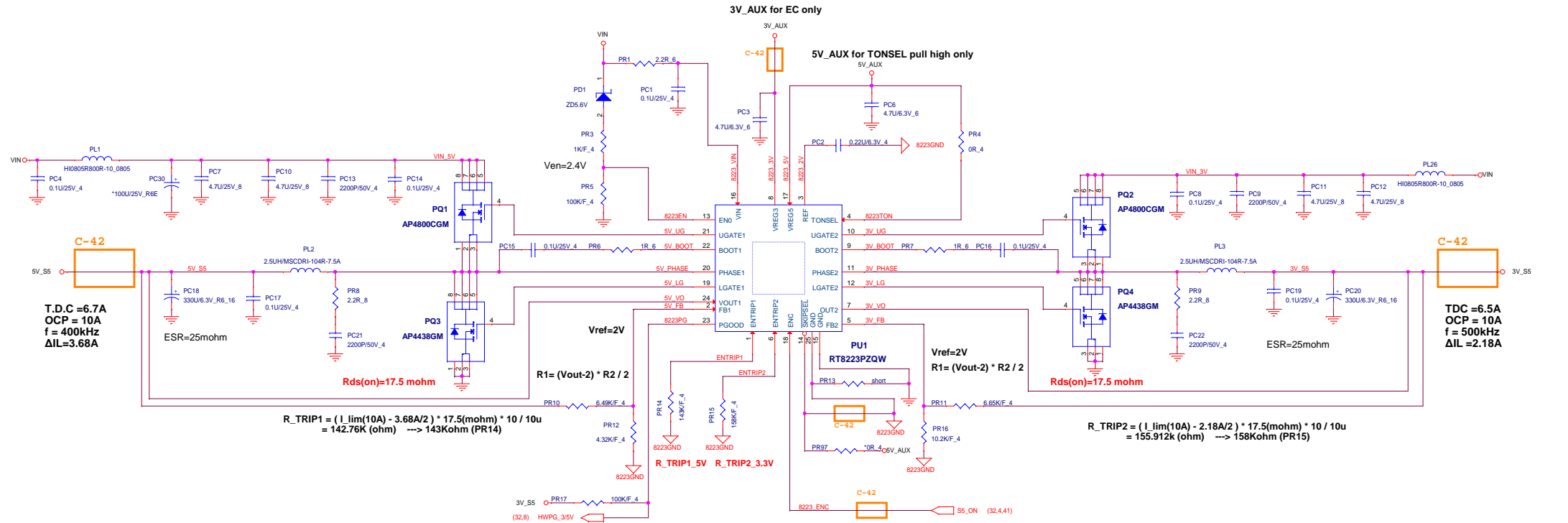


HOLE



Decoupling Cap





$\text{Irripple} = (\text{Vin} - \text{Vout}) \cdot \text{Vout} / (\text{Vin} \cdot \text{L} \cdot \text{f})$

O.C.P setup information

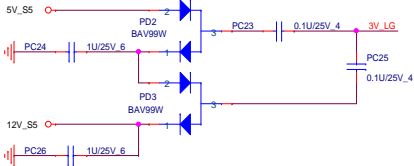
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
5V	17.5m_Max	10	3.68	400	2.5uH	143K
3.3V	17.5m_Max	10	2.18	500	2.5uH	158K

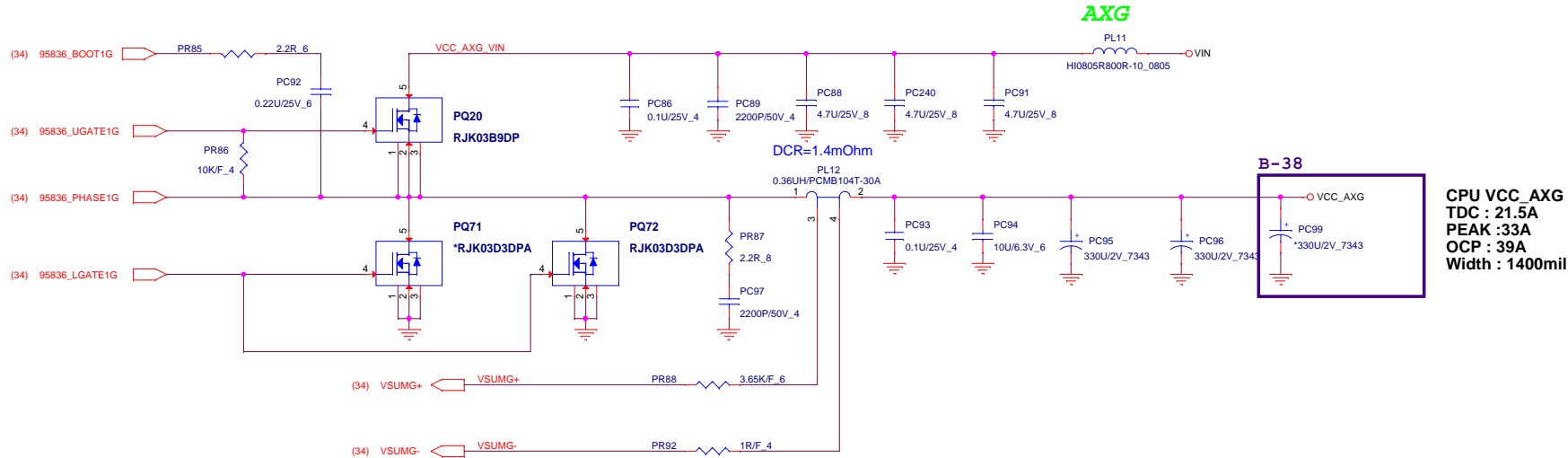
L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max
Si4134DY	SO-8	9.9A/14A	17.5m
AO4712	SO-8	10A/11.2A	18.0m
AO4710	SO-8	11A/12.7A	14.2m
AP4438GSM	SO-8	7A/11.7A	18.0m
DMG4812	SO-8	9.6A/10.7A	18.5m
AON7702	DFN3x3	11A/20A	14.0m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON






CPU VCC_AXG
TDC : 21.5A
PEAK :33A
OCP : 39A
Width : 1400mil

Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7X7X4	ETQP4LR36AFM

L/S Mosfet parameter

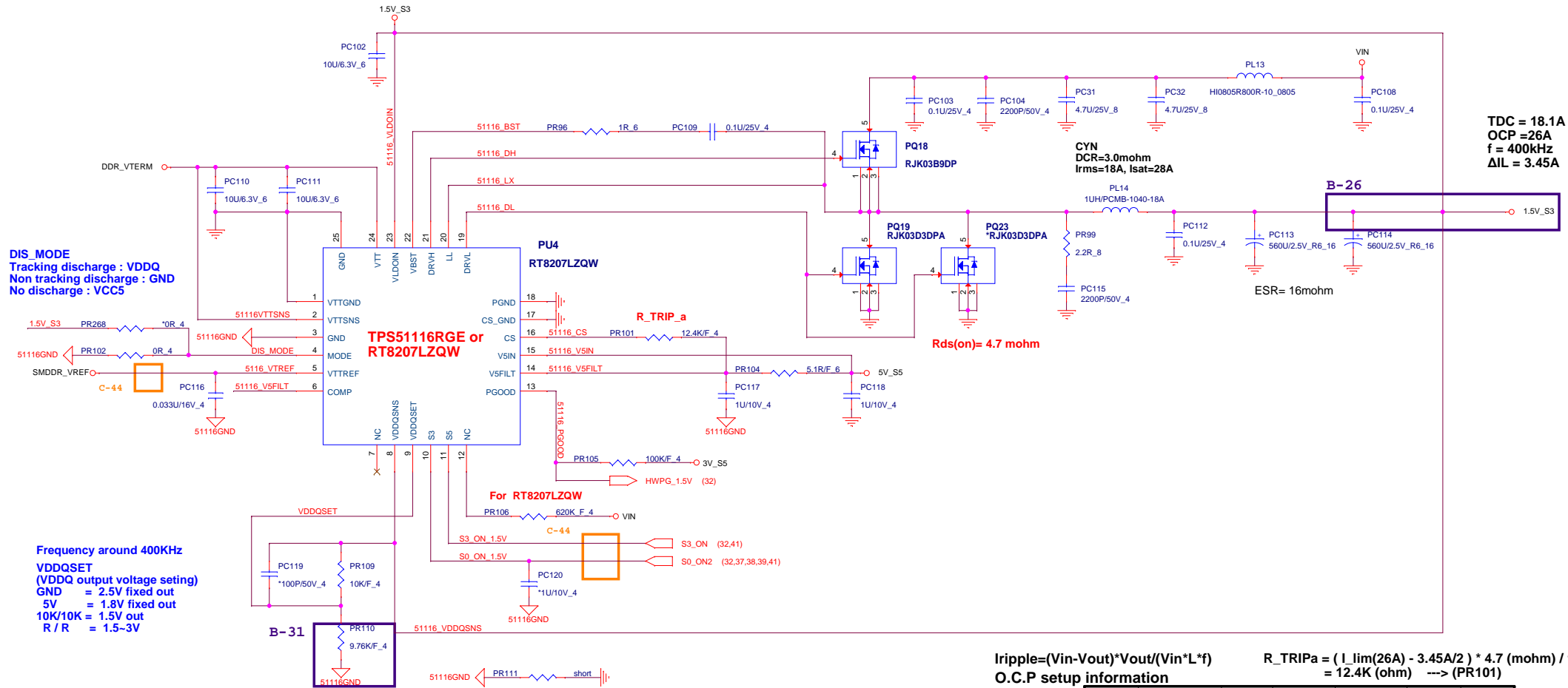
Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES



Quanta Computer Inc.
PROJECT : FH6T
CPU GFX (ISL95836HRTZ-T)

Size	Document Number	Rev 1A
Date: Thursday, December 13, 2012	Sheet 35 of 45	

DDR3 1.5V_S3 (TPS5116RGE or RT8207LZQW)


$$R_TRIPa = (I_lim(26A) - 3.45A/2) * 4.7 \text{ (mohm)} / 10u$$

$$= 12.4K \text{ (ohm)} \rightarrow (PR101)$$

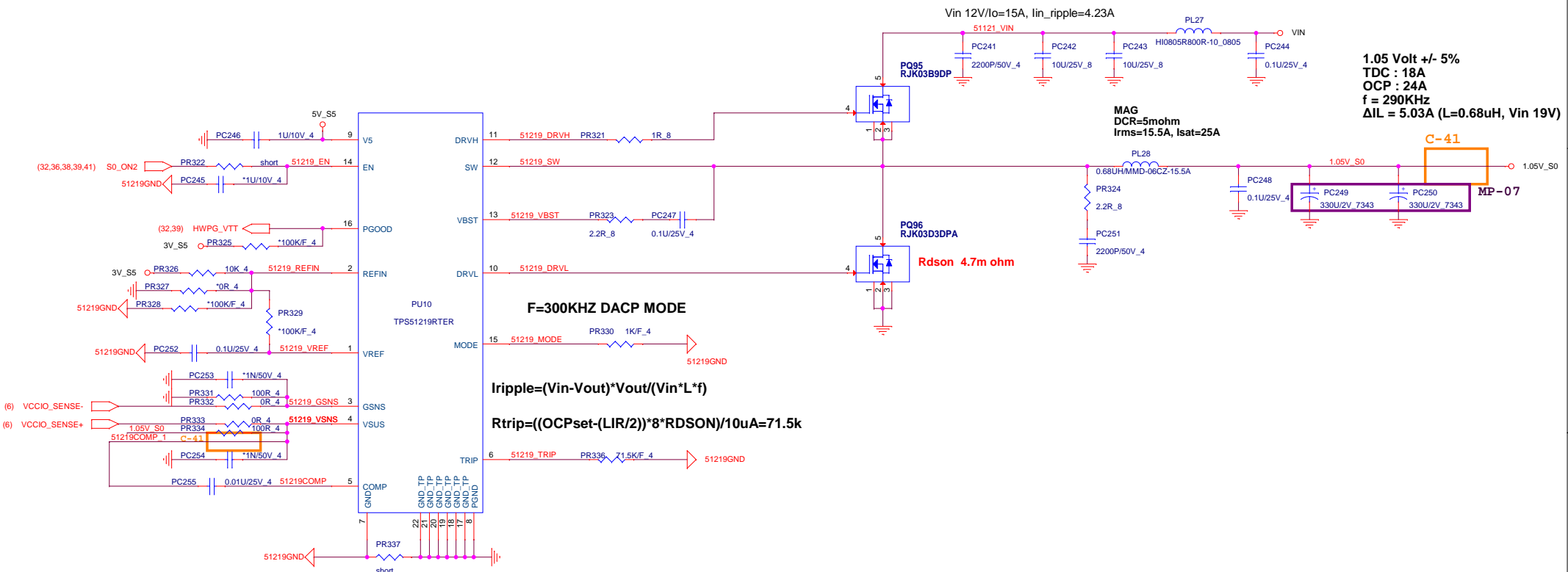
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.5V	4.7m_Max	26	3.45	400	1uH	12.4K

L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

Inductor information

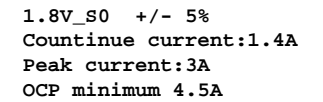
Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

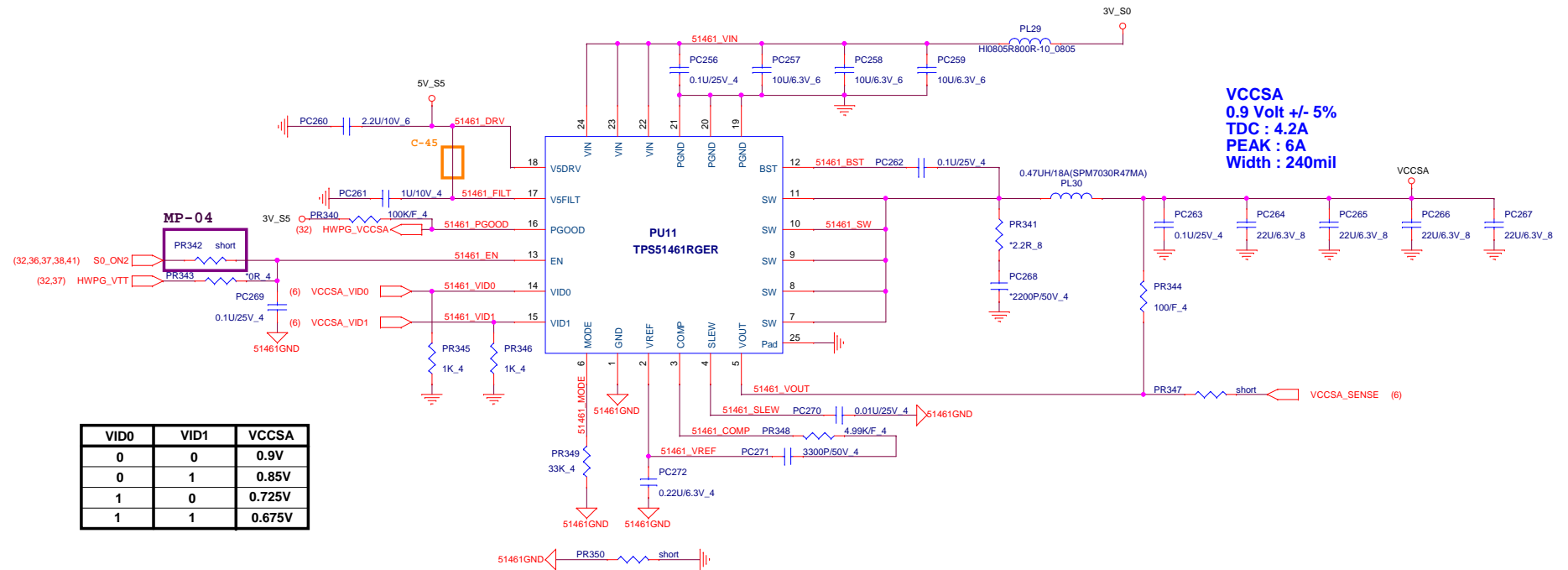


Output Voltage Selection	
RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjustable from VREF

Inductor information						
Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

O.C.P setup information						
Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	24	3.306	300	1uH	56.2K

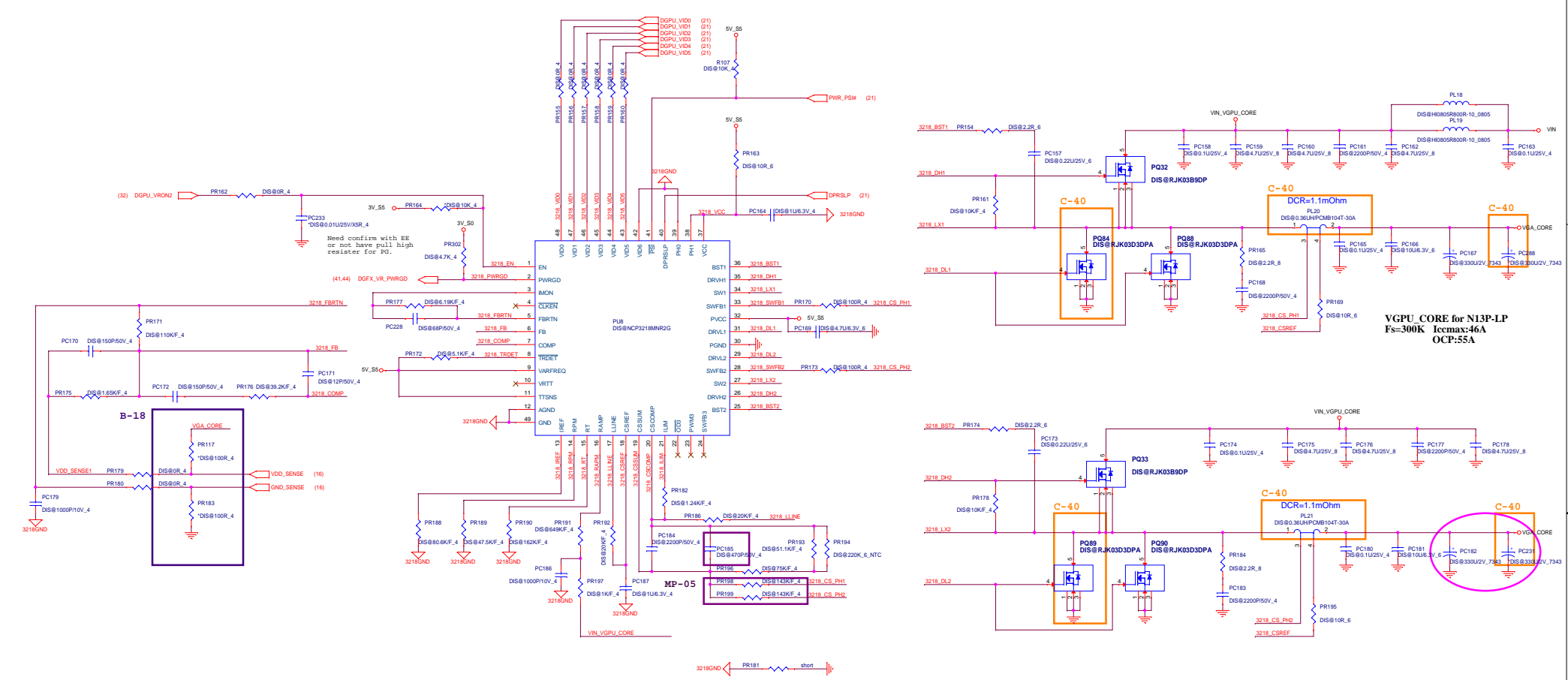




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L/S Mosfet parameter

Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

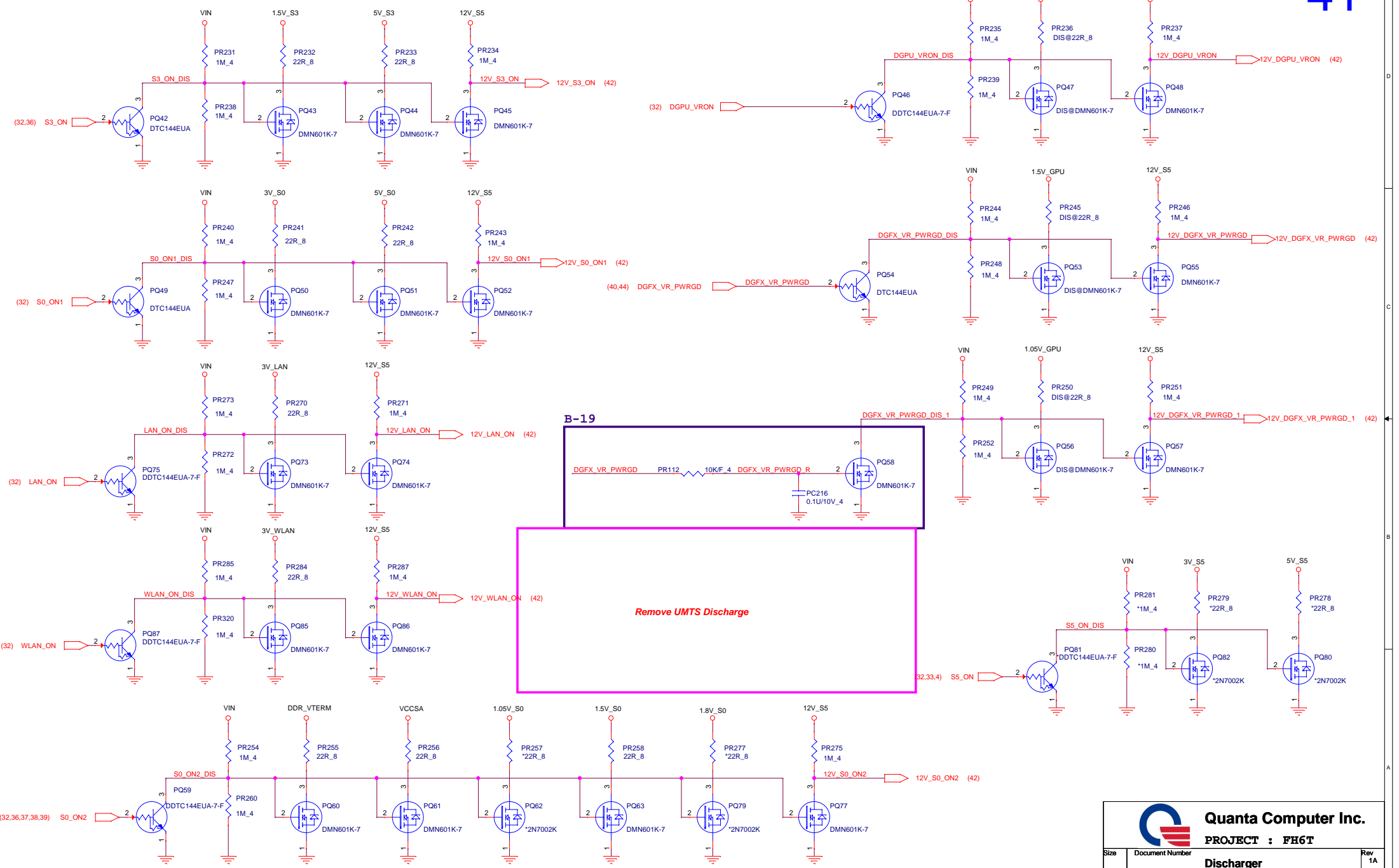
Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	20	25	1.2m Max.	7x7x3	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7x7x3	ETQP4LR36AFM

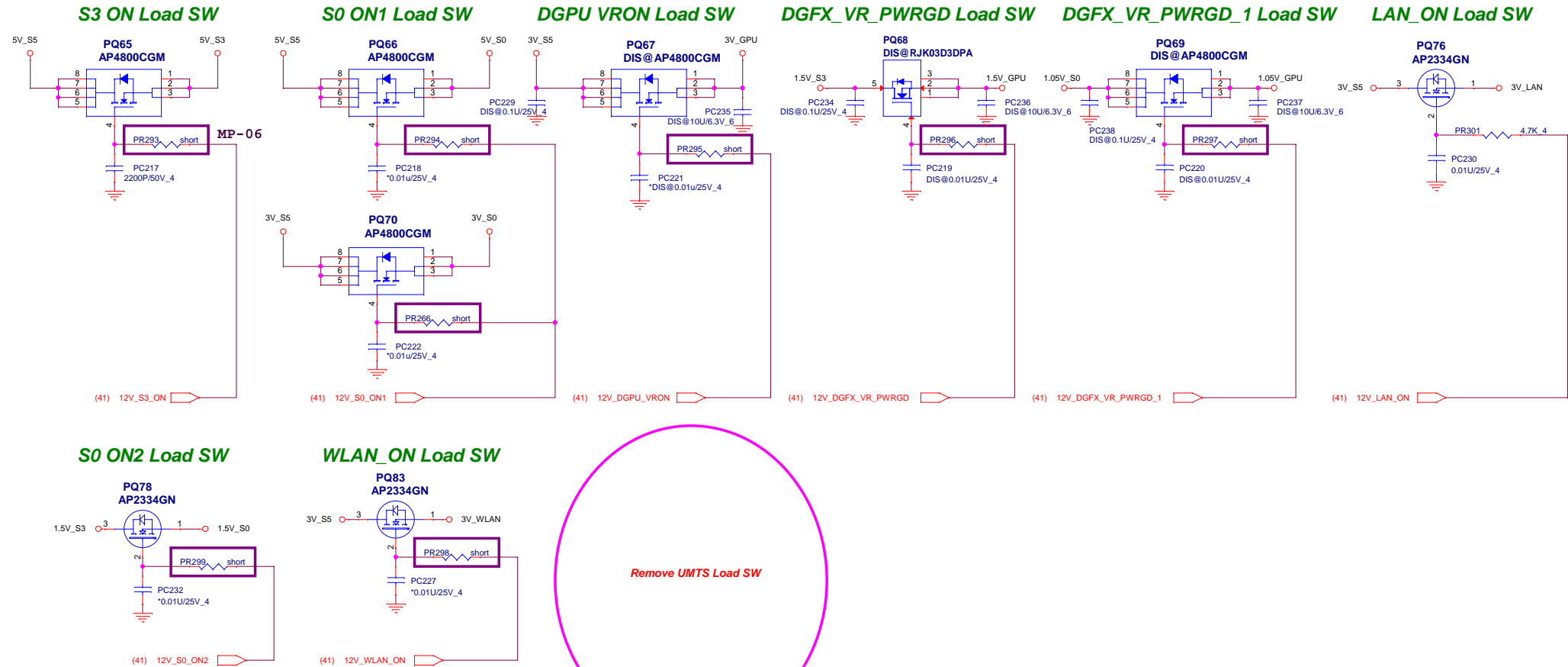
VGPU_CORE for N13P-LP
Fs=300K Iccmax:46A
OCP:55A

Power rail discharge

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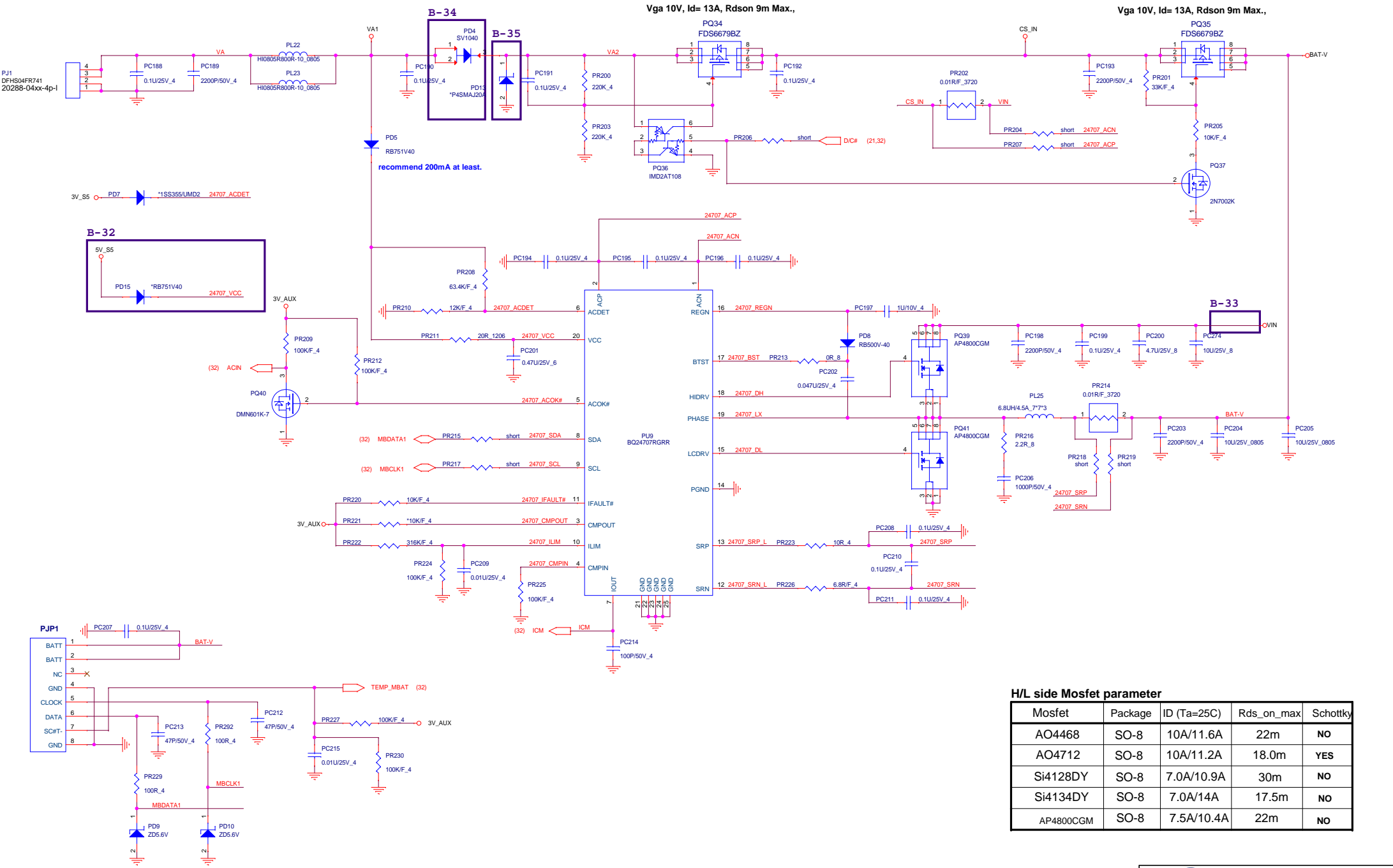


Load Switch



Mosfet parameter


Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	8.4A/10.4A	22m	+/- 20V
AP4800CGM	SO-8	7.5A/10.4A	22m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP2334GN	SOT-23	4.5A/5.0A	42m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V



H/L side Mosfet parameter				
Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO
AP4800CGM	SO-8	7.5A/10.4A	22m	NO

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PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
A	01	-		1st Release
B	02	-		A - B
C	03	-	Dec/22/12'	B - C
MP				C - MP1


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